

# Specification Sheet

**Model No. :** ZJY105

**Description :** 1.69inch OLED Screen resolution 160\*128  
Size:39.9\*34\*1.7mm Driver Chip SEPS525 interface SPI 35Pin  
Voltage 12.5V Font Color Option 262,144Colors ZJY105

***Revised History***

Part Number	Revision	Revision Content	Revised on
ZJY105	A	New	Aug 01, 2006

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# 1. Basic Specifications

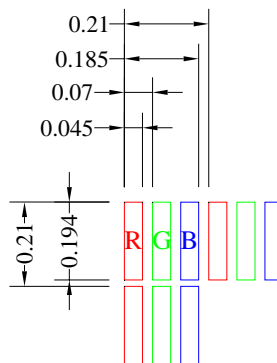
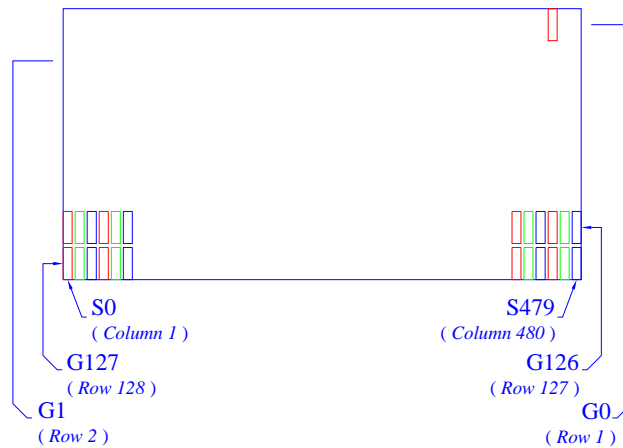
## 1.1 Display Specifications

- 1) Display Mode: Passive Matrix
- 2) Display Color: 262,144 Colors (Maximum)
- 3) Drive Duty: 1/128 Duty

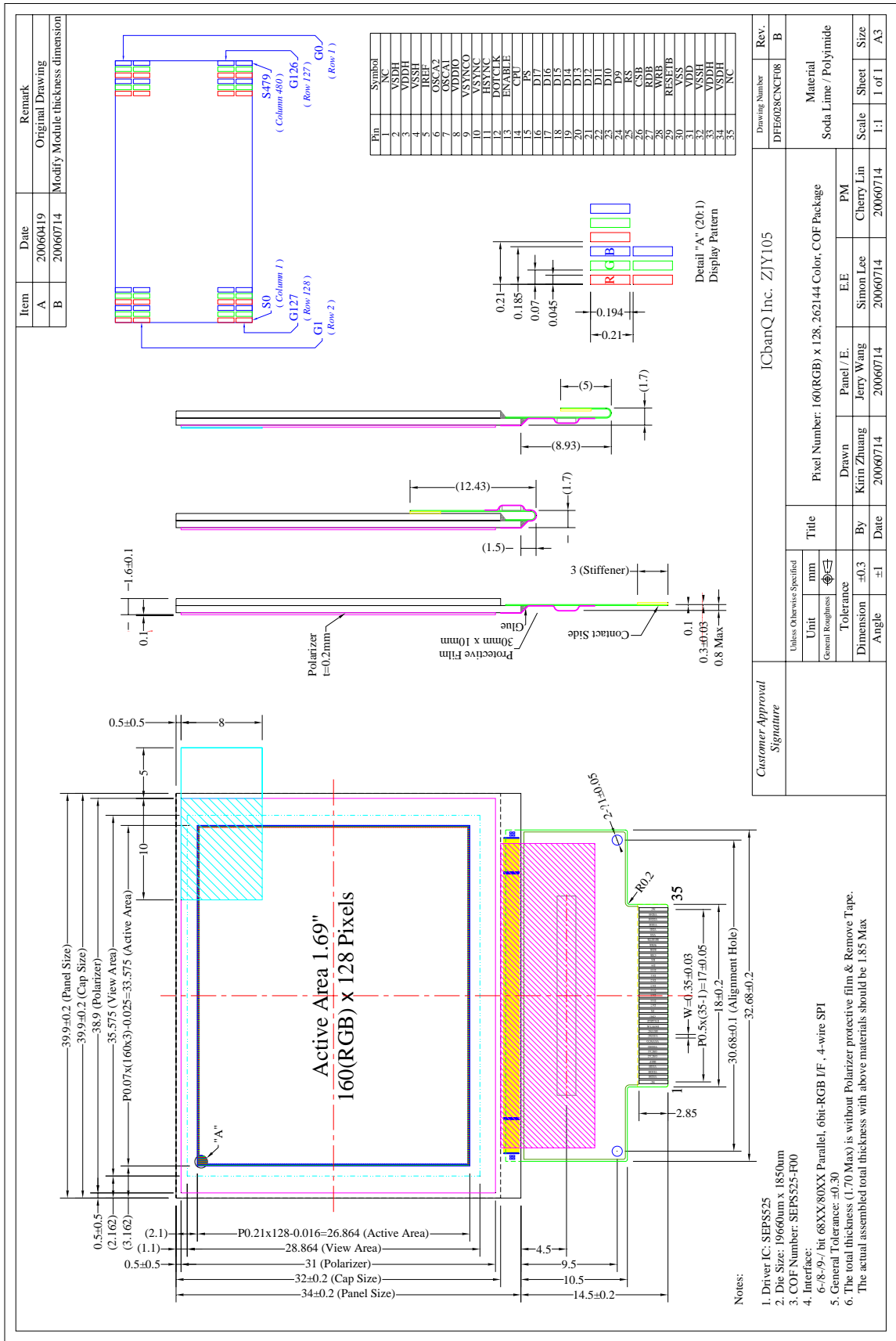
## 1.2 Mechanical Specifications

- 1) Outline Drawing: According to the annexed outline drawing number
- 2) Number of Pixels: 160 (RGB) × 128
- 3) Panel Size: 39.90 × 34.00 × 1.70 (mm)
- 4) Active Area: 33.575 × 26.864 (mm)
- 5) Pixel Pitch: 0.07 × 0.21(mm)
- 6) Pixel Size: 0.045 × 0.194 (mm)
- 7) Weight: 4.5 (g)

## 1.3 Active Area & Pixel Construction



# 1.4 Mechanical Drawing



## 1.5 Pin Definition

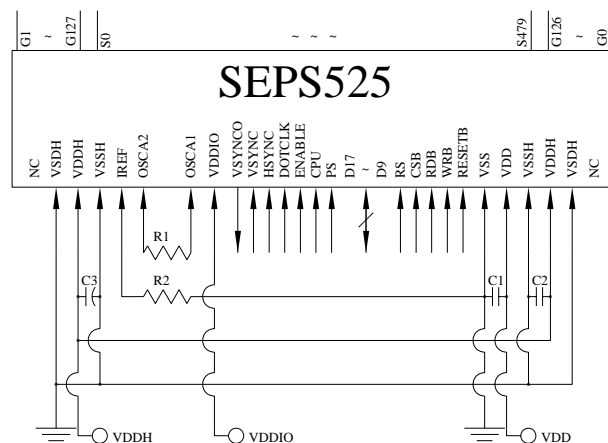
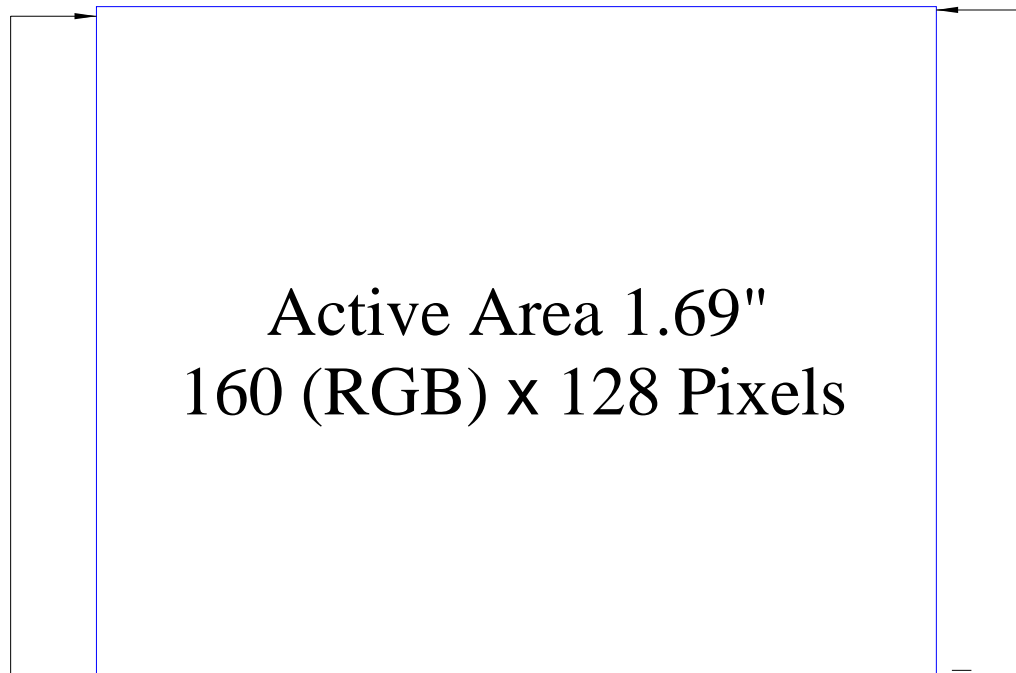
Pin Number	Symbol	Type	Function						
<i>Power Supply Pins</i>									
4,32	VSDH	P	<i>Data Driver Ground</i>						
2,33	VSSH	P	<i>Scan Driver Ground</i>						
3,34	VDDH	P	<i>Data, Scan Driver Power Supply.</i>						
30	VSS	P	<i>Logic Ground</i>						
31	VDD.	P	<i>Logic Power Supply.</i>						
8	VDDIO	P	<i>MPU I/F PAD Power Supply</i>						
<i>System Control Pins</i>									
5	IREF	I	<i>Current Reference for Brightness Adjustment</i> Tie 68K $\Omega$ resistor to VSS.						
6	OSCA2	O	<i>Fine adjustment for oscillation</i> Tie 10 K $\Omega$ resistor to OSCA1 between OSCA2.						
7	OSCA1	I	When the external clock mode is selected, OSCA1 is used external clock input.						
14	CPU	I	<i>Selects the CPU type</i> Low: 80-series CPU, High: 68-Series CPU.						
15	PS	I	<i>Selects parallel/Serial interface type</i> Low: serial, High: parallel.						
<i>MPU Interface Pins</i>									
9	VSYNCO	O	<i>RGB Mode Functional Pins</i> VSYNCO: Vertical Sync. Output VSYNC: Vertical Sync. Input HSYNC: Horizontal Sync. Input DOTCLK: Dot Clock Input ENABLE: Video Enable Input						
10	VSYNC	I							
11	HSYNC	I							
12	DOTCLK	I							
13	ENABLE	I							
16~24	D17~D9	I/O	<p><i>Host Data Input/Output Bus</i> These pins are 9-bit bi-directional data bus to be connected with MCU data bus.</p> <table border="1"> <thead> <tr> <th>PS</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>8_bit bus : D[17:10] 9_bit bus : D[17:9]</td> </tr> <tr> <td>0</td> <td>D[17] SCL : Synchronous clock input D[16] SDI : Serial data input D[15] SDO : Serial data output</td> </tr> </tbody> </table> <p>Fix unused pins to the VSS level.</p>	PS	Description	1	8_bit bus : D[17:10] 9_bit bus : D[17:9]	0	D[17] SCL : Synchronous clock input D[16] SDI : Serial data input D[15] SDO : Serial data output
PS	Description								
1	8_bit bus : D[17:10] 9_bit bus : D[17:9]								
0	D[17] SCL : Synchronous clock input D[16] SDI : Serial data input D[15] SDO : Serial data output								
25	RS	I	<i>Selects the data/command</i> Low: command, High: parameter/data						
26	CSB	I	<i>Chip Select</i> Low: SEPS525 is selected and can be accessed. High: SEPS525 is not selected and cannot be accessed.						
27	RDB	I	<i>Read or Read/Write Enable</i> 80-system bus interface: read strobe signal (active low). 68-system bus interface: bus enable strobe (active high). When serial mode, fix it to VDD or VSS level.						

### 1.5 Pin Definition (Continued)

Pin Number	Symbol	Type	Function
<i>MPU Interface Pins (Continued)</i>			
28	WRB	I	<i>Write or Read/Write Select</i> 80-system bus interface: write strobe signal (active low). 68-system bus interface: read/write select. Low: write, High: read. When serial mode, fix it to VDD or VSS level.
29	RESETB	I	<i>Chip Reset</i> Reset SEPS525 (active low)
<i>Reserved Pins</i>			
1,35	NC	-	<i>No Connection</i>



## 1.6 Block Diagram



MCU Interface Selection: PS, CPU

Pins connected to MCU interface: D17~D9, RS, CSB, RDB, WRB, RESETB, ENABLE, DOTCLK, HSYNC, and VSYNC

\* When RGB mode is used, D[17:12], ENABLE, DOTCLK, HSYNC, and VSYNC should follow the 6-bit RGB interface instruction. Otherwise, ENABLE, DOTCLK, HSYNC, and VSYNC these four input signal should be tie to VSS level, and VSYNCO should be floating.

C1: 1 $\mu$ F  
 C2, C3: 4.7 $\mu$ F  
 R1: 10k $\Omega$   
 R2: 68k $\Omega$

## 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	VDD	-0.3	4	V	1, 2
Supply Voltage for I/O Pins	VDDIO	-0.3	4	V	1, 2
Driver Supply Voltage	VDDH	-0.3	19.5	V	1, 2
Operating Temperature	T <sub>OP</sub>	-30	70	°C	-
Storage Temperature	T <sub>STG</sub>	-40	80	°C	-

Note 1: All the above voltages are on the basis of “GND = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

### 3. *Electrical Characteristics*

#### 3.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		2.6	2.8	3.3	V
Supply Voltage for I/O Pins	VDDIO		1.6	2.8	3.3	V
Driver Supply Voltage	VDDH		13.5	<u>14.0</u>	14.5	V
High Level Input	V <sub>IH</sub>		0.8×VDD	-	VDD	V
Low Level Input	V <sub>IL</sub>		0	-	0.4	V
High Level Output	V <sub>OH</sub>		VDD-0.4	-	-	V
Low Level Output	V <sub>OL</sub>		-	-	0.4	V

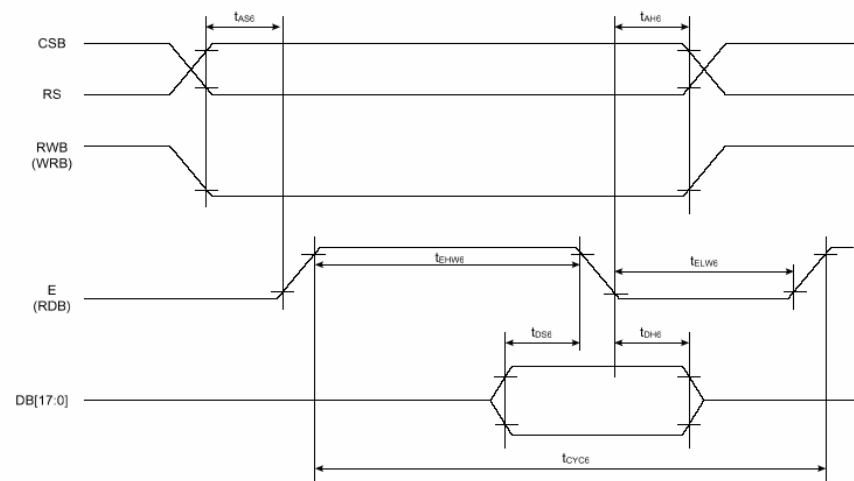
## 3.2 AC Characteristics

### 3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

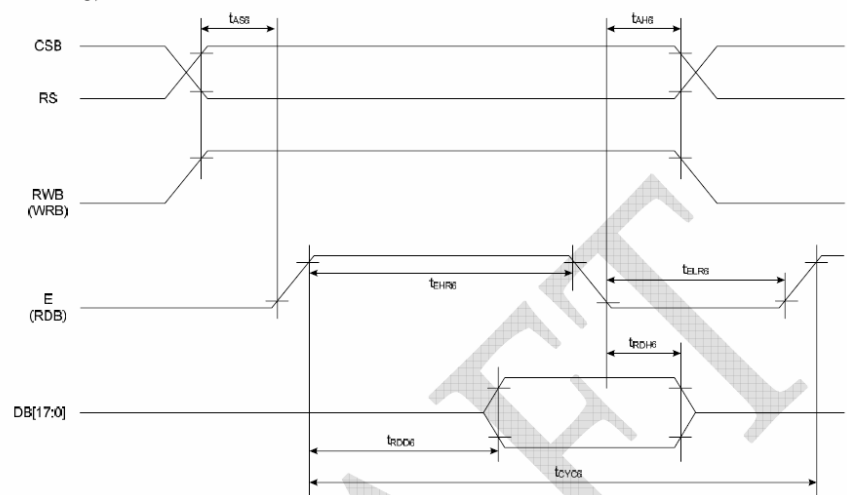
(VDD = 2.8V, Ta = 25°C)

Item	Symbol	Condition	Min	Max	Unit	Port
<i>Write Timing</i>						
Address hold timing	$t_{AH6}$	-	5	-	ns	CSB
Address setup timing	$t_{AS6}$	-	5	-	ns	RS
System cycle timing	$t_{CYC6}$	-	100	-	ns	E
Write "L" pulse width	$t_{ELW6}$	-	45	-	ns	E
Write "H" pulse width	$t_{EHW6}$	-	45	-	ns	E
Data setup timing	$t_{DS6}$	-	40	-	ns	DB[17:0]
Data hold Timing	$t_{DH6}$	-	10	-	ns	DB[17:0]
<i>Read Timing</i>						
Address hold timing	$t_{AH6}$	-	10	-	ns	CSB
Address setup timing	$t_{AS6}$	-	10	-	ns	RS
System cycle timing	$t_{CYC6}$	-	200	-	ns	E
Read "L" pulse width	$t_{ELR6}$	-	90	-	ns	E
Read "H" pulse width	$t_{EHR6}$	-	90	-	ns	E
Read data output delay time	$t_{RDD6}$	-				
Data hold Timing						

( Write Timing )



( Read Timing )



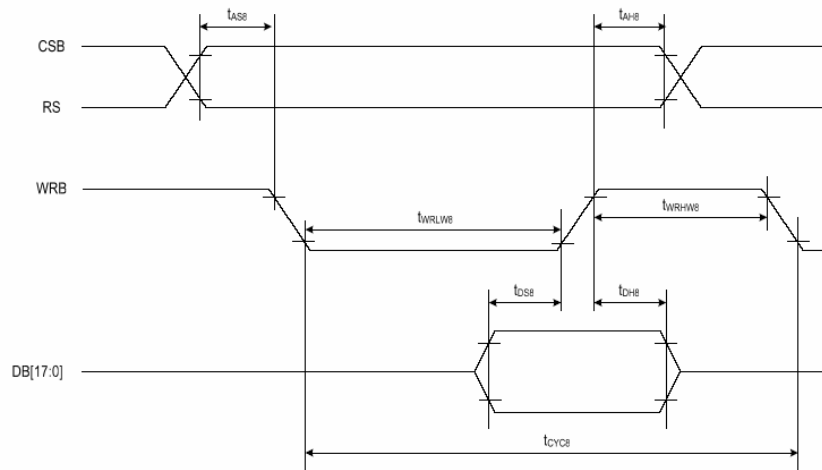
### 3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25°C)

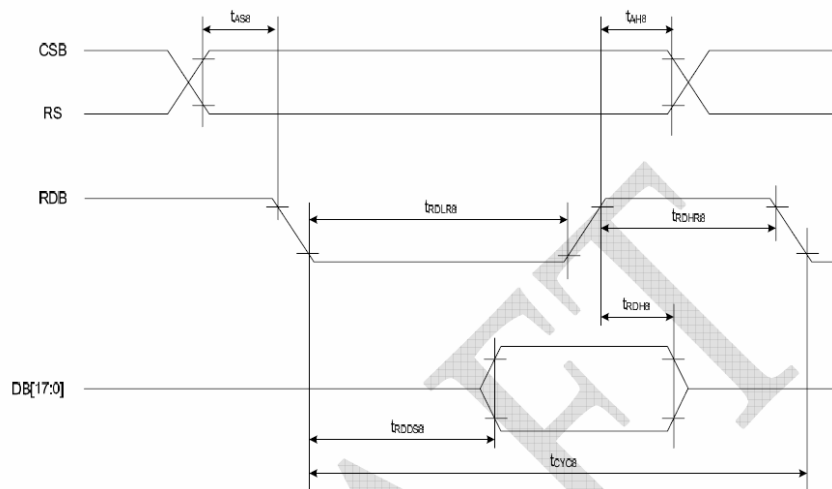
Item	Symbol	Condition	Min	Max	Unit	Port
<i>Write Timing</i>						
Address hold timing	$t_{AH8}$	-	5	-	ns	CSB
Address setup timing	$t_{AS8}$	-	5	-	ns	RS
System cycle timing	$t_{CYC8}$	-	100	-	ns	WRB
Write "L" pulse width	$t_{WRLW8}$	-	45	-	ns	WRB
Write "H" pulse width	$t_{WRHW8}$	-	45	-	ns	WRB
Data setup timing	$t_{DS8}$	-	30	-	ns	DB[17:0]
Data hold Timing	$t_{DH8}$	-	10	-	ns	DB[17:0]
<i>Read Timing</i>						
Address hold timing	$t_{AH8}$	-	10	-	ns	CSB
Address setup timing	$t_{AS8}$	-	10	-	ns	RS
System cycle timing	$t_{CYC8}$	-	200	-	ns	RDB
Read "L" pulse width	$t_{RDLR8}$	-	90	-	ns	RDB
Read "H" pulse width	$t_{RDHR8}$	-	90	-	ns	RDB
Read data output delay time	$t_{RDD8}$	$C_L = 15pF$	-	60	ns	DB[17:0]
Data hold Timing	$t_{RDH8}$	$C_L = 15pF$	0	-	ns	DB[17:0]

\*) All the timing reference is 10% and 90% of VDD.

( Write Timing )



( Read Timing )

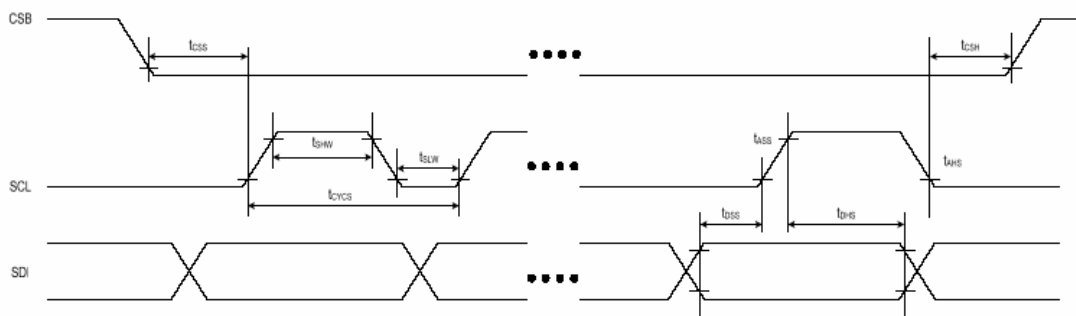


### 3.2.3 Serial Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25°C)

Item	Symbol	Condition	Min	Max	Unit	Port
Serial clock cycle	$t_{CYCS}$		60			
SCL "H" pulse width	$t_{SHW}$	-	25	-	ns	SCL
SCL "L" pulse width	$t_{SLW}$		25			
Data setup timing	$t_{DSS}$	-	25	-	ns	SDI
Data hold Timing	$t_{DHS}$		25			
CSB-SCL timing	$t_{CSS}$		25	-	ns	CSB
CSB-hold timing	$t_{CSH}$		25			

\*) All the timing reference is 10% and 90% of VDD.



### 3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L <sub>br</sub>	Note 3	70	100	-	cd/m <sup>2</sup>
C.I.E. (White)	(x)	Note 3	0.22	0.26	0.30	
	(y)		0.24	0.28	0.32	
C.I.E. (Red)	(x)	Note 3	0.61	0.65	0.69	
	(y)		0.30	0.34	0.38	
C.I.E. (Green)	(x)	Note 3	0.26	0.30	0.34	
	(y)		0.58	0.62	0.66	
C.I.E. (Blue)	(x)	Note 3	0.10	0.14	0.18	
	(y)		0.15	0.19	0.23	
Dark Room Contrast	CR		-	>1000:1	-	
View Angle			>160	-	-	degree

Note3: Optical measurement with polarizer is taken @ VDD, VDDIO = 2.8V, VDDH = 14V, and the software initial setting with section 4.4.2 Reference Parameter Table for Normal Operation Mode.

### 3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		2.4	2.8	3.3	V
Supply Voltage for I/O Pins	VDDIO		1.6	2.8	3.3	V
Driver Supply Voltage	VDDH		13.5	14.0	14.5	V
Operating Current for VDD	I <sub>VDD</sub>	Note 4	-	2.5	3.5	mA
		Note 5	-	2.5	3.5	mA
Operating Current for VDDH	I <sub>VDDH</sub>	Note 4	-	25	31	mA
		Note 5	-	8	10	mA
Sleep Mode Current for VDD	I <sub>VDD, SLEEP</sub>		-	1	5	μA
Sleep Mode Current for VDDH	I <sub>VDDH, SLEEP</sub>		-	1	5	μA

Note 4: VDD & VDDIO = 2.8V, VDDH = 14V, L<sub>br</sub> @ 100cd/m<sup>2</sup>, full white with polarizer, software initial setting follow section 4.4.2 Reference Parameter Table for Normal Operation Mode.

Note 5: VDD & VDDIO = 2.8V, VDDH = 14V, L<sub>br</sub> @ 30cd/m<sup>2</sup>, full white with polarizer, software initial setting follow section 4.4.2 Reference Parameter Table for Power Saving Mode.

## 4. Functional Specification

### 4.1. Commands

Refer to the Technical Manual for the SEPS525

### 4.2 Power down and Power up Sequence

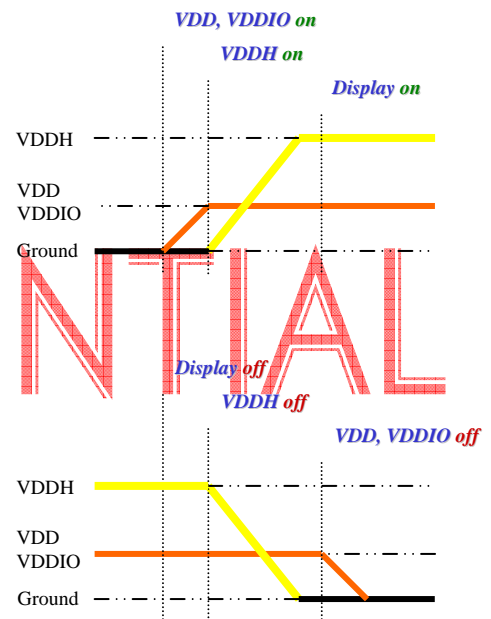
To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

#### 4.2.1 Power up Sequence:

1. Power up VDD, VDDIO
2. Send Display off command
3. Clear Screen
4. Power up VDDH
5. Delay 100ms  
(when VDD is stable)
6. Send Display on command

#### 4.2.2 Power down Sequence:

1. Send Display off command
2. Power down VDDH
3. Delay 100ms  
(when VDDH is reach 0 and  
panel is completely discharges)
4. Power down VDD, VDDIO



### 4.3 Reset Circuit

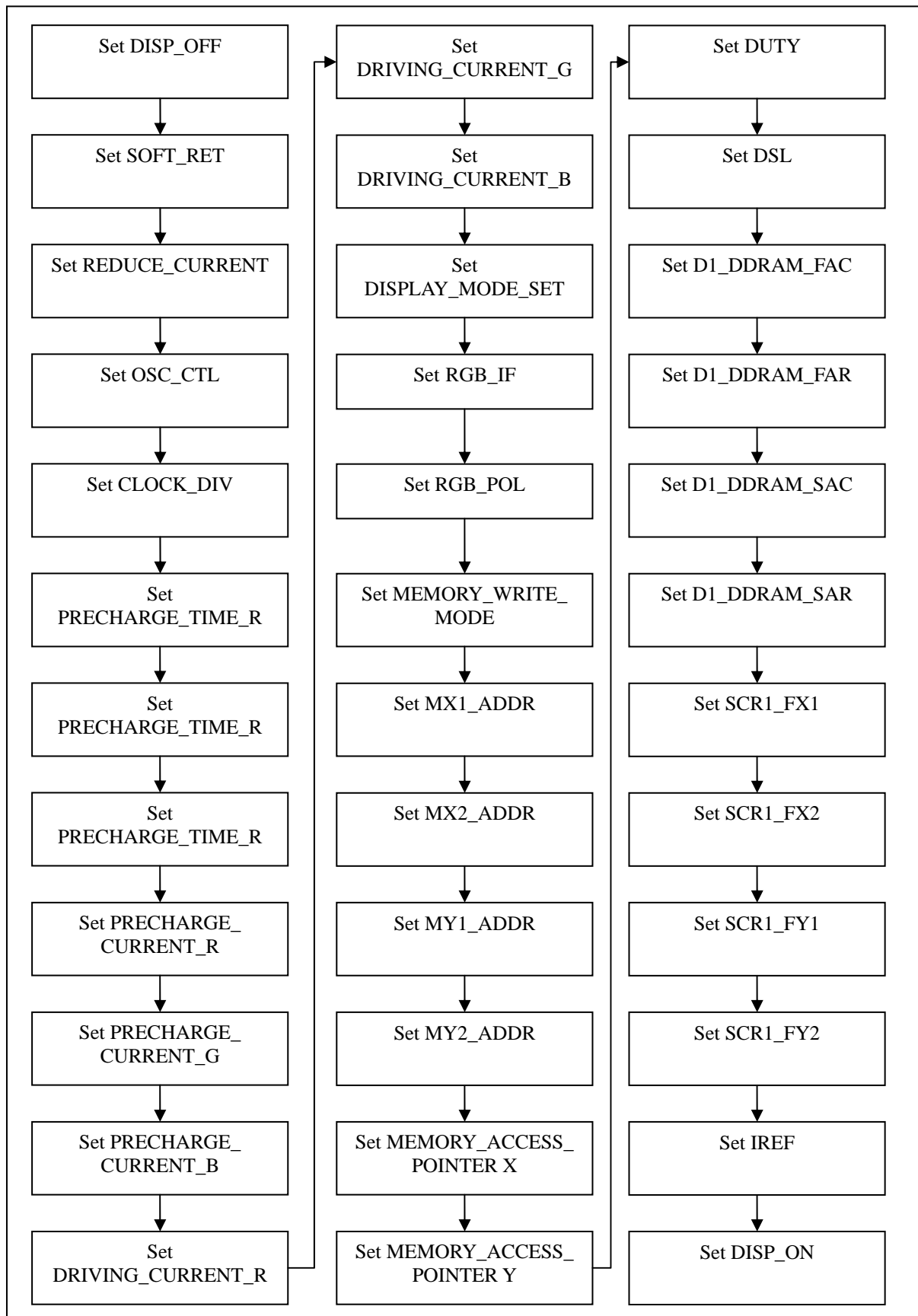
When RESETB input is low, the chip is initialized with the following status:

1. Frame frequency: 90Hz
2. OSC: internal OSC
3. Internal OSC: ON
4. DDRAM write horizontal address: MX1 = 00h, MX2 = 9Fh
5. DDRAM write vertical address: MY1 = 00h, MY2 = 7Fh
6. Display data RAM write: HC = 1, VC = 1, HV = 0
7. RGB data swap: OFF
8. Row scan shift direction: G0, G1, ... , G126, G127
9. Column data shift direction: S0, S1, ... , S478, S479
10. Display ON/OFF: OFF
11. Panel display size: FX1 = 00h, FX2 = 9Fh, FY1 = 00h, FY2 = 7Fh
12. Display data RAM read column/row address: FAC = 00h, FAR = 00h
13. Precharge time(R/G/B): 0 clock
14. Precharge current(R/G/B): 0 uA
15. Driving current(R/G/B): 0 uA



## 4.4 Actual Application Example

### 4.4.1 Driver IC Initial Setting Flowchart



#### 4.4.2 Reference Parameters Table

(VDD = 2.8V, Ta = 25°C)

Command Parameter	Normal Operation Mode	Power Saving Mode
Set Display On_OFF	0x06 , 0x00	
Set SOFT_RST	0x05 , 0x00	
Set REDUCE_CURRENT	0x04 , 0x01 wait 1ms	0x04,0x00
Set OSC_CTL	0x02 , 0x01	
Set CLOCK_DIV	0x03 , 0x09	
Set PRECHARGE_TIME_R	0x08 , 0x03	0x08 , 0x00
Set PRECHARGE_TIME_G	0x09 , 0x05	0x09 , 0x00
Set PRECHARGE_TIME_B	0x0A , 0x05	0x0A , 0x00
Set PRECHARGE_CURRENT_R	0x0B , 0x56	0x0B , 0x00
Set PRECHARGE_CURRENT_G	0x0C , 0x4D	0x0C , 0x00
Set PRECHARGE_CURRENT_B	0x0D , 0x46	0x0D , 0x00
Set DRIVING_CURRENT_R	0x10 , 0x0A	0x10 , 0x0D
Set DRIVING_CURRENT_G	0x11 , 0x0A	0x11 , 0x0C
Set DRIVING_CURRENT_B	0x12 , 0x0A	0x12 , 0x0B
Set DISPLAY_MODE_SET	0x13 , 0x00	
Set RGB_IF	0x14 , 0x01	
Set RGB_POL	0x15 , 0x00	
Set MEMORY_WRITE_MODE	0x16 , 0x76	
Set MX1_ADDR	0x17 , 0x00	
Set MX2_ADDR	0x18 , 0x9F	
Set MY1_ADDR	0x19 , 0x00	
Set MY2_ADDR	0x1A , 0x7F	
Set MEMORY_ACCESS_POINTER X	0x20 , 0x00	
Set MEMORY_ACCESS_POINTER Y	0x21 , 0x00	
Set DUTY	0x28 , 0x7F	
Set DSL	0x29 , 0x00	
Set D1_DDRAM_FAC	0x2E , 0x00	
Set D1_DDRAM_FAR	0x2F , 0x00	
Set D1_DDRAM_SAC	0x31 , 0x00	
Set D1_DDRAM_SAR	0x32 , 0x00	
Set SCR1_FX1	0x33 , 0x00	
Set SCR1_FX2	0x34 , 0x9F	
Set SCR1_FY1	0x35 , 0x00	
Set SCR1_FY2	0x36 , 0x7F	
Set IREF	0x80 , 0x00	
Set DISP_ON_OFF	0x06 , 0x01	

## 5. Reliability

### 5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 1 hr dwell	

\* The samples used for the above tests do not include polarizer.

\* No moisture condensation is observed during tests.

### 5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	Hrs	70 cd/m <sup>2</sup> , 50% checkerboard	6
Storage Life Time	20,000	-	Hrs	Ta=25°C, 50%RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

### 5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

## 6. Outgoing Quality Control Specifications

### 6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

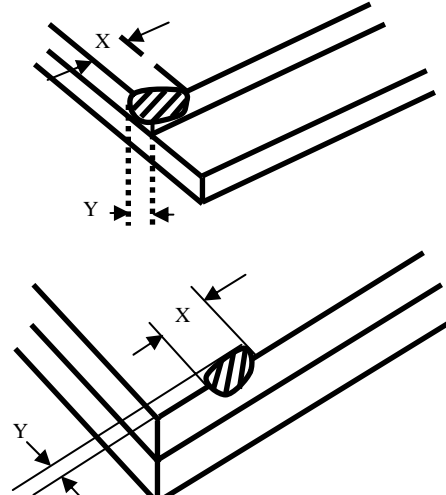
### 6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

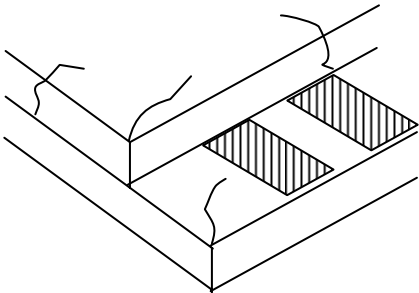

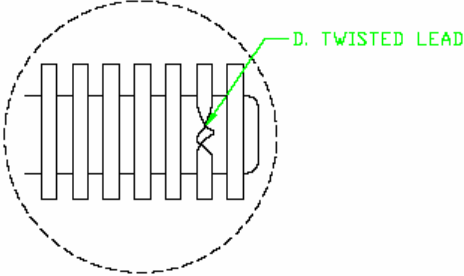
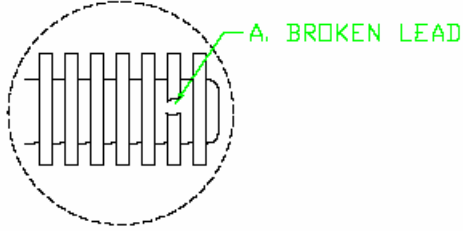
### 6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

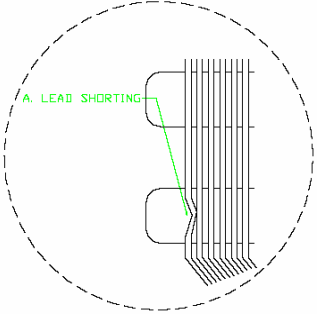
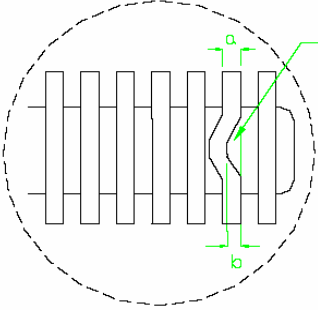
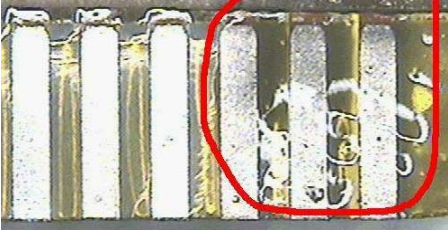
#### 6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	<p>X &gt; 6 mm (Along with Edge) Y &gt; 1 mm (Perpendicular to edge)</p> 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

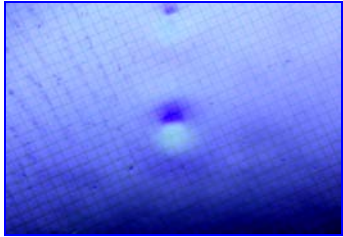
Check Item	Classification	Criteria
Panel Crack	Minor	<p>Any crack is not allowable.</p>  <p>A 3D perspective diagram of a rectangular panel with a crack running along one of its edges. The crack is shown as a jagged line extending across the surface of the panel.</p>
Copper Exposed (Even Pin or Film)	Minor	<p>Not Allowable by Naked Eye Inspection</p>
Film or Trace Damage	Minor	 <p>A close-up photograph of a yellow printed circuit board (PCB) showing a circular hole or damage in the copper film or trace area.</p>
Terminal Lead Twist	Minor	<p>Not Allowable</p>  <p>A diagram showing a row of vertical terminal leads. One lead is twisted, indicated by a green arrow and the label "D. TWISTED LEAD". The entire row is enclosed in a dashed circle.</p>
Terminal Lead Broken	Minor	<p>Not Allowable</p>  <p>A diagram showing a row of vertical terminal leads. One lead is broken, indicated by a green arrow and the label "A. BROKEN LEAD". The entire row is enclosed in a dashed circle.</p>
Terminal Lead Probe Mark	Acceptable	<p>Ok</p>

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	<p>NG if any bent lead cause lead shorting.</p> 
	Minor	<p>NG for horizontally bent lead more than 50% of its width.</p> 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

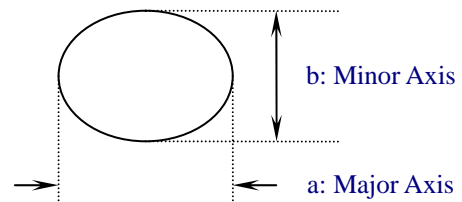
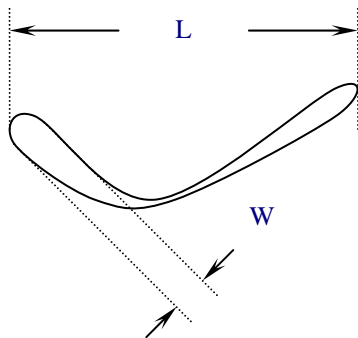
### 6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

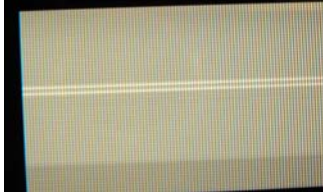
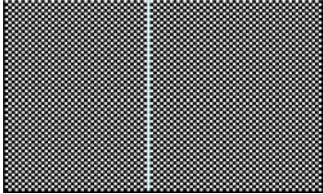
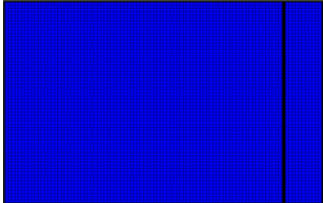
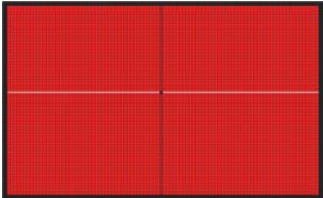
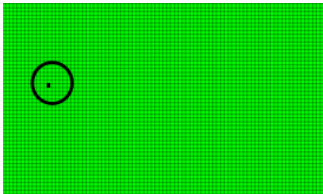
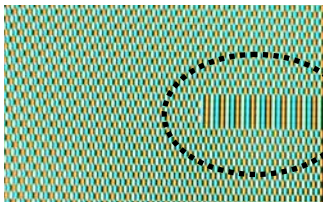
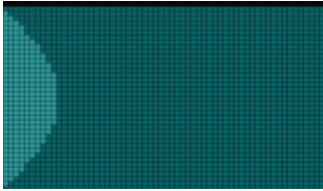
Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for Any
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1, L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
		$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dirt, Spot-Shape Defect (On Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	
Fingerprint, Flow Mark (On Polarizer)	Minor	Not allowable

\* Protective film should not be tear off when cosmetic check.

\*\* Definition of W & L &  $\Phi$  (Unit: mm):  $\Phi = (a + b) / 2$

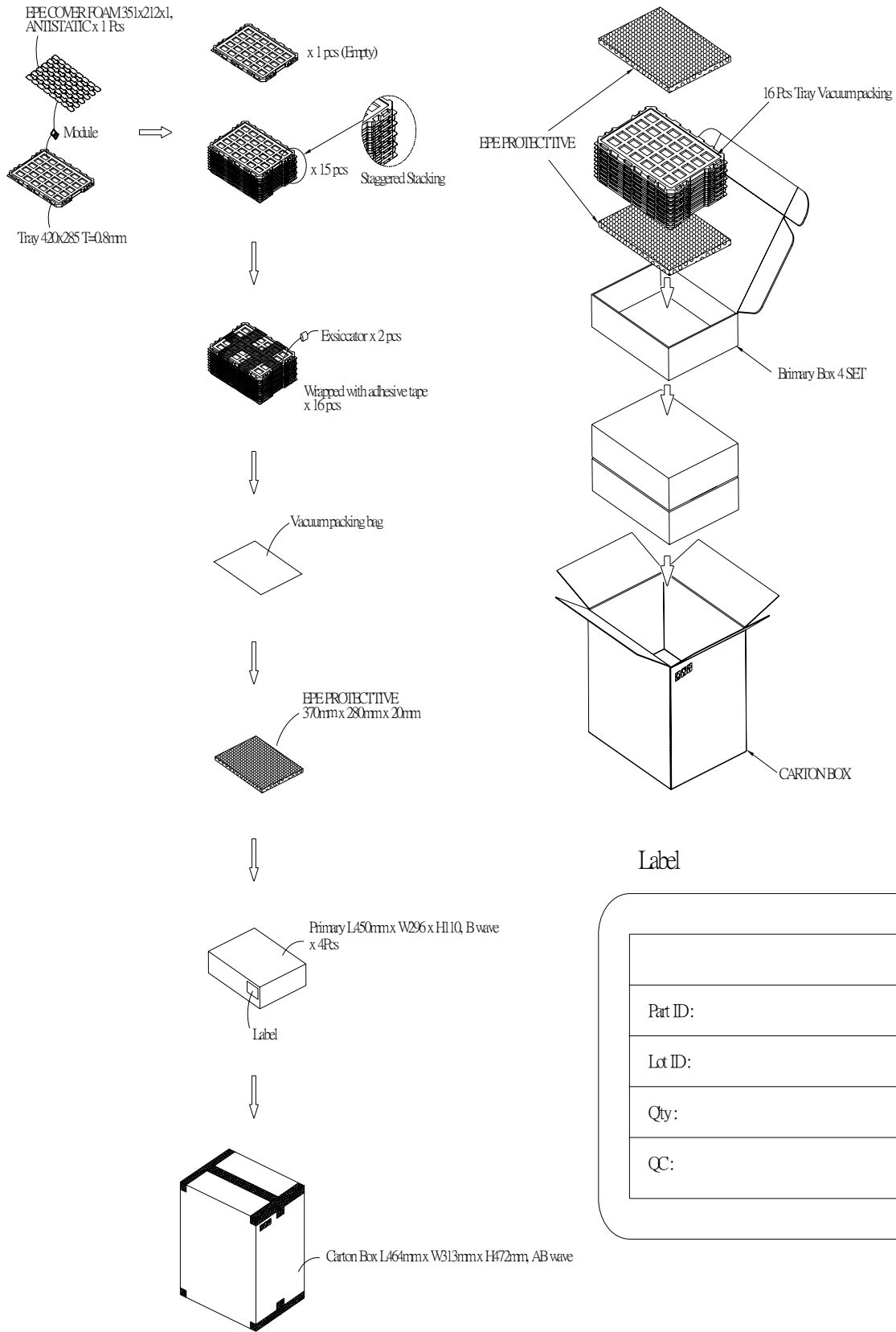


### 6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not allowable
Bright Line	Major	
Missed Line	Major	 
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major	



## 7. Package Specifications



Label

Part ID:
Lot ID:
Qty:
QC:

## **8. Precautions When Using These OEL Display Modules**

### **8.1 Handling Precautions**

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display area, both of top and back sides, or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to touch these sections on carrying and assembly.
- 4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
- 5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
  - \* Scotch Mending Tape No. 810 or an equivalentNever try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

Also, pay attention that the following liquid and solvent may spoil the polarizer:

  - \* Water
  - \* Ketone
  - \* Aromatic Solvents
- 6) When installing the OEL display module, be careful not to apply twisting stress or deflection stress to the OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
- 7) Do not apply stress to the LSI chips and the surrounding molded sections.
- 8) Do not disassemble nor modify the OEL display module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handling OEL display modules to prevent occurrence of element breakage accidents by static electricity.
  - \* Be sure to make human body grounding when handling OEL display modules.
  - \* Be sure to ground tools to use or assembly such as soldering irons.
  - \* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
  - \* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
- 11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
- 12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

## 8.2 Storage Precautions

- 1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)  
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
- 2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

## 8.3 Designing Precautions

- 1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OEL display module, fasten the external plastic housing section.
- 7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSPS525  
\* Connection (contact) to any other potential than the above may lead to rupture of the IC.

## 8.4 Precautions when disposing of the OEL display modules

- 1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

## 8.5 Other Precautions

- 1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal

state can be restored. Also, there will be no problem in the reliability of the module.

- 2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
  - \* Pins and electrodes
  - \* Pattern layouts such as the COF
- 3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
  - \* Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
  - \* Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
- 4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.