Specification Sheet

Model No. : ZJY101

Description : 1.45inch OLED Screen resolution 160*128 Size:35.8*30.8*1.7mm Driver Chip SEPS525 interface SPI 35Pin Voltage V Font Color Option 262,144Colors ZJY101

Revised History

Part Number	Revision	Revision Content	Revised on
ZJY101	A	New	Apr 11, 2006

Contents

1. *Basic Specifications*

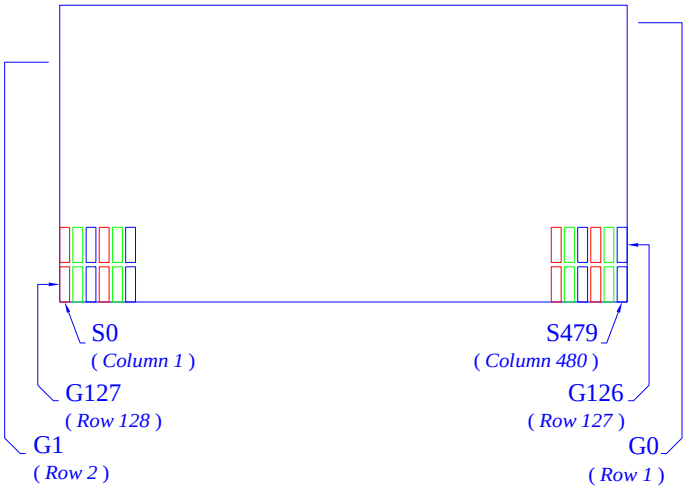
1.1 Display Specifications

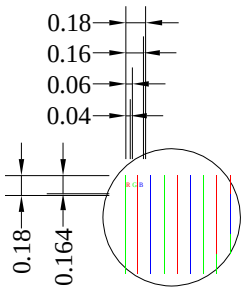
1) Display Mode: Passive Matrix
2) Display Color: 262,144 Colors (Maximum)
3) Drive Duty: 1/128 Duty

1.2 Mechanical Specifications

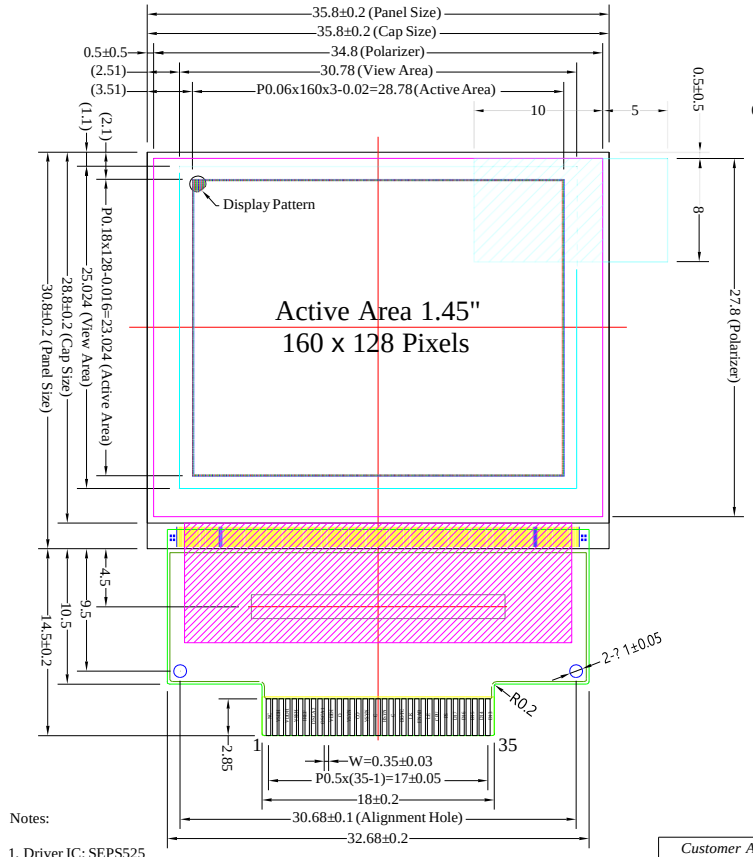
1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 160 (RGB) × 128
3) Panel Size: 35.80 × 30.80 × 1.7 (mm)
4) Active Area: 28.78 × 23.024 (mm)
5) Pixel Pitch: 0.06 × 0.18 (mm)
6) Pixel Size: 0.04 × 0.164 (mm)
7) Weight: 3.6 (g)

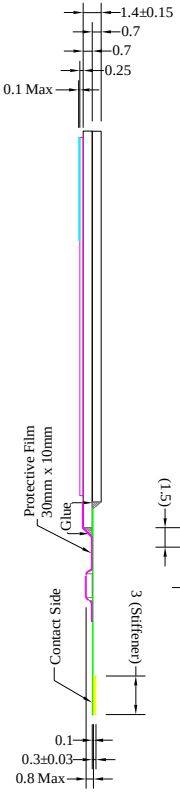
1.3 Active Area & Pixel Construction

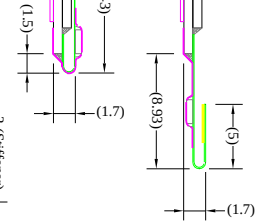


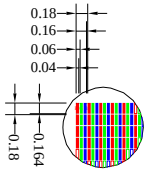


Item	Date	Remark
A	20060320	Original Drawing

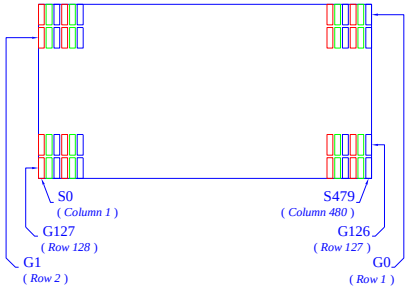








Detail "A" (5:1)
Display Pattern



Pin	Symbol
1	NC
2	VSDH
3	VDDH
4	VSSH
5	IREF
6	OSCA2
7	OSCA1
8	VDDIO
9	VSYNCO
10	VSYNC
11	HSYNC
12	DOTCLK
13	ENABLE
14	CPU
15	PS
16	D17
17	D16
18	D15
19	D14
20	D13
21	D12
22	D11
23	D10
24	D9
25	RS
26	CSB
27	RDB
28	WRB
29	RESETB
30	VSS
31	VDD
32	VSSH
33	VDDH
34	VSDH
35	NC

Notes:

1. Driver IC: SEPS525
2. Die Size: 19660um x 1850um
3. COF Number: SEPS525F
4. Interface:
   6-/8-/9-/ bit, RGB I/F 68XX/80XX Parallel, 4-wire SPI
5. General Tolerance: ±0.30
6. The total thickness (1.55 Max) is without Polarizer.
   The actual assembled total thickness with above materials should be 1.90 Max

Customer Approval Signature	ICbanQ Inc. ZJY101						Drawing Number		Rev.
							DFE6028CNCF06		A
	Unless Otherwise Specified		Title	Pixel Number: 160(RGB) x 128, 262144 Color, COF Package			Material		
	Unit	mm					Soda Lime / Polyimide		
	General Roughness								
	Tolerance			Drawn	Checked	Reviewed	PM			
	Dimension	±0.3	By	Kirin Zhuang	Jerry Wang	Ray Tso	Jian Jia Hung	Scale	Sheet	Size
	Angle	±1	Date	20060320	20060320	20060320	20060320	1:1	1 of 1	A3

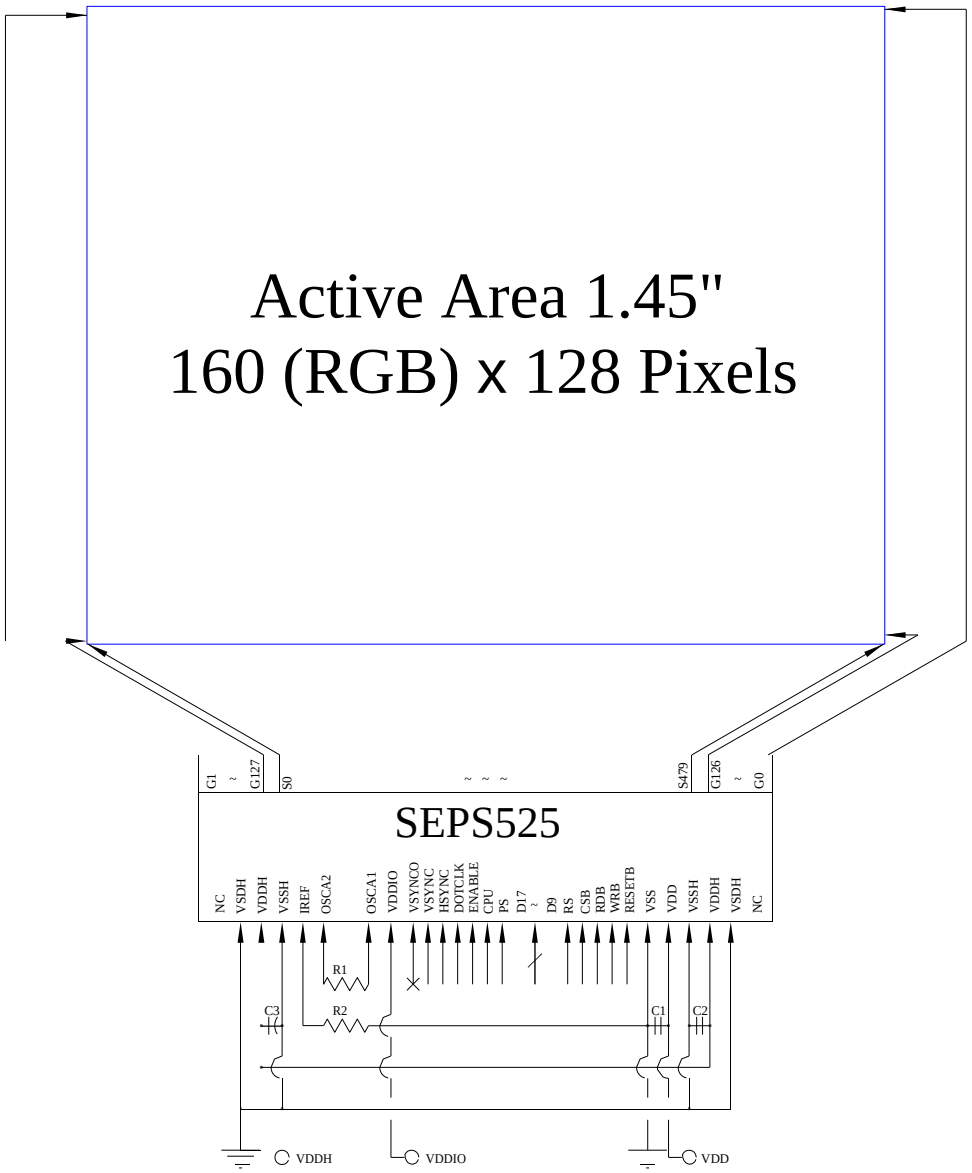
1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Type</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply Pins</td></tr>
<tr><td>4,32</td><td>VSDH</td><td>P</td><td>Data Driver Ground</td></tr>
<tr><td>2,33</td><td>VSSH</td><td>P</td><td>Scan Driver Ground</td></tr>
<tr><td>3,34</td><td>VDDH</td><td>P</td><td>Data, Scan Driver Power Supply.</td></tr>
<tr><td>30</td><td>VSS</td><td>P</td><td>Power Supply Ground</td></tr>
<tr><td>31</td><td>VDD.</td><td>P</td><td>Logic Power Supply.</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td>MPU I/F PAD Power Supply</td></tr>
<tr><td colspan="4">System Control Pins</td></tr>
<tr><td>5</td><td>IREF</td><td>I/O</td><td>Current Reference for Brightness Adjustment
Tie 70KΩ resistor to VSS.</td></tr>
<tr><td>6</td><td>OSCA2</td><td>O</td><td rowspan="2">Fine adjustment for oscillation
Tie 10 KΩ resistor to OSCA1 between OSCA2.
When the external clock mode is selected, OSCA1 is used external clock input.</td></tr>
<tr><td>7</td><td>OSCA1</td><td>I</td></tr>
<tr><td>14</td><td>CPU</td><td>I</td><td>Selects the CPU type
Low: 80-series CPU, High: 68-Series CPU.</td></tr>
<tr><td>15</td><td>PS</td><td>I</td><td>Selects parallel/Serial interface type
Low: serial, High: parallel.</td></tr>
<tr><td colspan="4">MPU Interface Pins</td></tr>
<tr><td>9</td><td>VSYNCO</td><td>O</td><td rowspan="5">RGB Mode Functional Pins
VSYNCO: Vertical Sync. Output
VSYNC: Vertical Sync. Input
HSYNC: Horizontal Sync. Input
DOTCLK: Dot Clock Input
ENABLE: Video Enable Input</td></tr>
<tr><td>10</td><td>VSYNC</td><td>I</td></tr>
<tr><td>11</td><td>HSYNC</td><td>I</td></tr>
<tr><td>12</td><td>DOTCLK</td><td>I</td></tr>
<tr><td>13</td><td>ENABLE</td><td>I</td></tr>
<tr><td>16~24</td><td>D17~D9</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 9-bit bi-directional data bus to be connected with MCU data bus.
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>1</td><td>8_bit bus : D[17:10]
9_bit bus : D[17:9]</td></tr>
<tr><td>0</td><td>D[17] SCL : Synchronous clock input
D[16] SDI : Serial data input
D[15] SDO : Serial data output</td></tr>
</table>
Fix unused pins to the VSS level.</td></tr>
<tr><td>25</td><td>RS</td><td>I</td><td>Selects the data/command
Low: command, High: parameter/data</td></tr>
<tr><td>26</td><td>CSB</td><td>I</td><td>Chip Select
Low: SEPS225 is selected and can be accessed.
High: SEPS225 is not selected and cannot be accessed.</td></tr>
<tr><td>27</td><td>RDB</td><td>I</td><td>Read or Read/Write Enable
80-system bus interface: read strobe signal (active low).
68-system bus interface: bus enable strobe (active high).
When serial mode, fix it to VDD or VSS level.</td></tr>
</table>

1.5 Pin Definition (Continued)

Pin Number	Symbol	Type	Function
MPU Interface Pins (Continued)			
28	WRB	I	*Write or Read/Write Select* 80-system bus interface: write strobe signal (active low). 68-system bus interface: read/write select. Low: write, High: read. When serial mode, fix it to VDD or VSS level.
29	RESETB	I	*Chip Reset* Reset SEPS225 (active low)
Reserved Pins			
1,35	NC	-	*No Connection*

1.6 Block Diagram



MCU Interface Selection: PS, CPU

Pins connected to MCU interface: D17~D9, RS, CSB, RDB, WRB, RESETB, ENABLE, DOTCLK, HSYNC, and VSYNC

* When RGB mode is used, D[17:12], ENABLE, DOTCLK, HSYNC, and VSYNC should follow the 6-bit RGB interface instruction. Otherwise, ENABLE, DOTCLK, HSYNC, and VSYNC these four input signal should be tie to VDDIO level.

C1:	1μF
C2, C3:	4.7μF
R1:	10kΩ
R2:	68kΩ

2. *Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	VDD	-0.3	4	V	1, 2
Supply Voltage for I/O Pins	VDDIO	-0.3	4	V	1, 2
Driver Supply Voltage	VDDH	-0.3	19.5	V	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. *Electrical Characteristics*

3.1 DC Characteristics

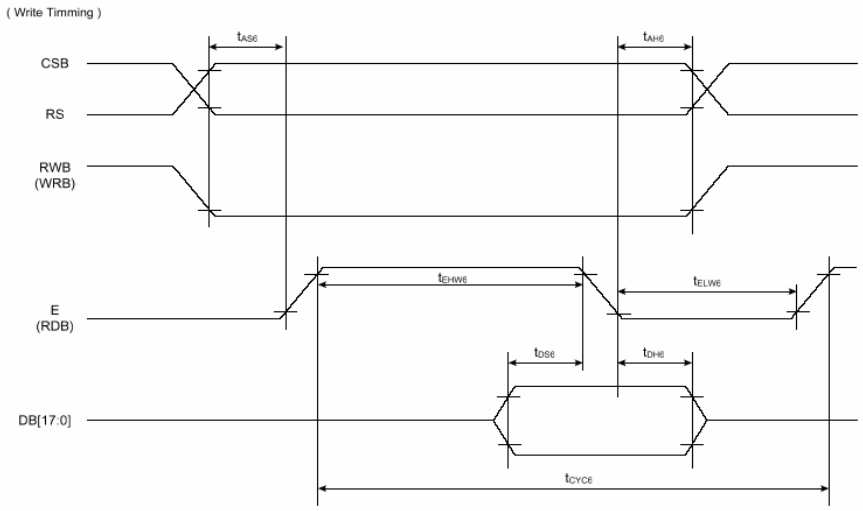
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		2.6	2.8	3.3	V
Supply Voltage for I/O Pins	VDDIO		1.6	2.8	3.3	V
Driver Supply Voltage	VDDH		-	13.0	-	V
High Level Input	V_{IH}		0.8×VDD	-	VDD	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH}		VDD-0.4	-	-	V
Low Level Output	V_{OL}		-	-	0.4	V

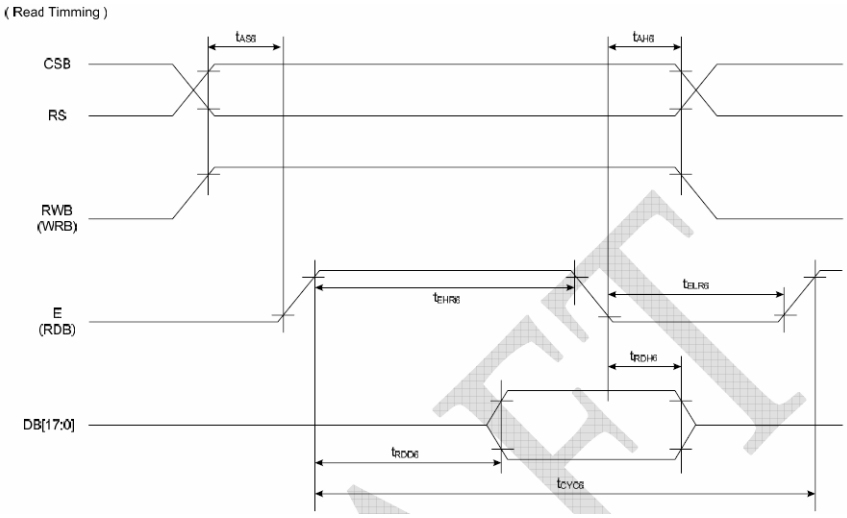
3.2 AC Characteristics

3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25℃)

Item	Symbol	Condition	Min	Max	Unit	Port
Write Timing						
Address hold timing Address setup timing	t_{AH6} t_{AS6}	-	5 5	-	ns	CSB RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW6}	-	100 45 45	-	ns	E
Data setup timing Data hold Timing	t_{DS6} t_{DH6}		40 10	-	ns	DB[17:0]
Read Timing						
Address hold timing Address setup timing	t_{AH6} t_{AS6}	-	10 10	-	ns	CSB RS
System cycle timing Read "L" pulse width Read "H" pulse width	t_{CYC6} t_{ELR6} t_{EHR6}	-	200 90 90	-	ns	E
Read data output delay time Data hold Timing	t_{RDD6}	C_L = 15pF	0	70	ns	DB[17:0]



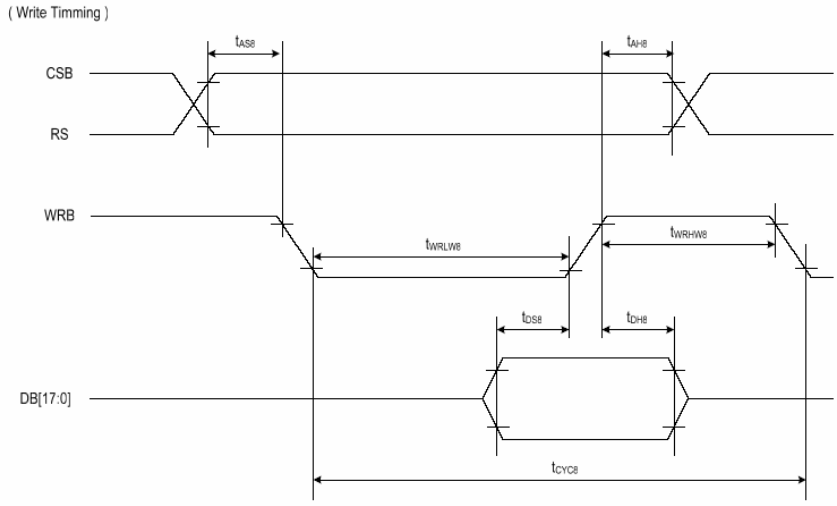


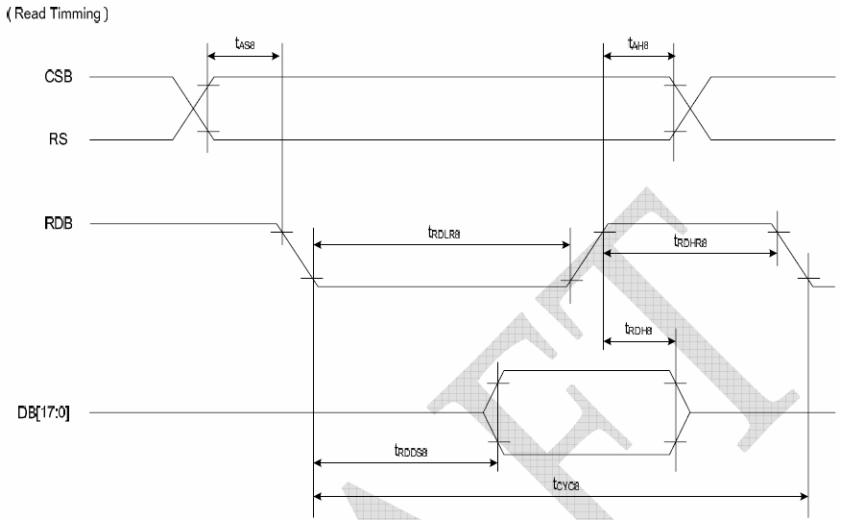
3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25°C)

Item	Symbol	Condition	Min	Max	Unit	Port
Write Timing						
Address hold timing Address setup timing	t_{AH8} t_{AS8}	-	5 5	-	ns	CSB RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}	-	100 45 45	-	ns	WRB
Data setup timing Data hold Timing	t_{DS8} t_{DH8}		30 10	-	ns	DB[17:0]
Read Timing						
Address hold timing Address setup timing	t_{AH8} t_{AS8}	-	10 10	-	ns	CSB RS
System cycle timing Read "L" pulse width Read "H" pulse width	t_{CYC8} t_{RDLR8} t_{RDHR8}	-	200 90 90	-	ns	RDB
Read data output delay time Data hold Timing	t_{RDD8} t_{RDH8}	C_L = 15pF	- 0	60	ns	DB[17:0]

*) All the timing reference is 10% and 90% of VDD.





3.2.3 Serial Interface Timing Characteristics:

(VDD = 2.8V, Ta = 25℃)

Item	Symbol	Condition	Min	Max	Unit	Port
Serial clock cycle	t_{CYCS}	-	60	-	ns	SCL
SCL "H" pulse width	t_{SHW}		25			
SCL "L" pulse width	t_{SLW}		25			
Data setup timing	t_{DSS}	-	25	-	ns	SDI
Data hold Timing	t_{DHS}		25			
CSB-SCL timing	t_{CSS}	-	25	-	ns	CSB
CSB-hold timing	t_{CSH}		25			

*) All the timing reference is 10% and 90% of VDD.