

Low Voltage Detectors ($V_{DF} = 0.8V \sim 1.5V$)
 Standard Voltage Detectors ($V_{DF} = 1.6V \sim 6.0V$)

GENERAL DESCRIPTION

The XC61C series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies.

Detect voltage is extremely accurate with minimal temperature drift.

Both CMOS and N-channel open drain output configurations are available.

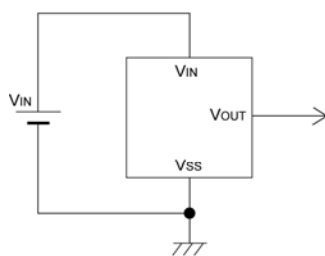
APPLICATIONS

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

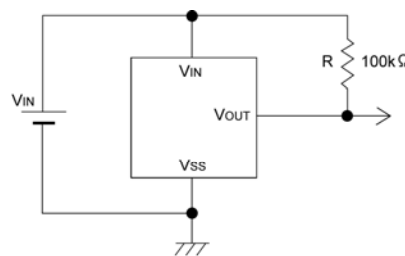
FEATURES

- Highly Accurate** : $\pm 2\%$
: $\pm 1\%$ (Standard Voltage VD: 2.6V~5.0V)
- Low Power Consumption** : $0.7 \mu A$ (TYP.) [$V_{IN} = 1.5V$]
- Detect Voltage Range** : $0.8V \sim 6.0V$ in $0.1V$ increments
- Operating Voltage Range** : $0.7V \sim 6.0V$ (Low Voltage)
 $0.7V \sim 10.0V$ (Standard Voltage)
- Detect Voltage Temperature Characteristics**
: $\pm 100ppm/^{\circ}C$ (TYP.)
- Output Configuration** : N-channel open drain or CMOS
- Packages** : SSOT-24
SOT-23
SOT-89
TO-92
- Environmentally Friendly** : EU RoHS Compliant, Pb Free

TYPICAL APPLICATION CIRCUITS

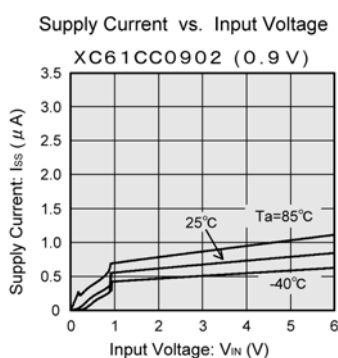


CMOS Output

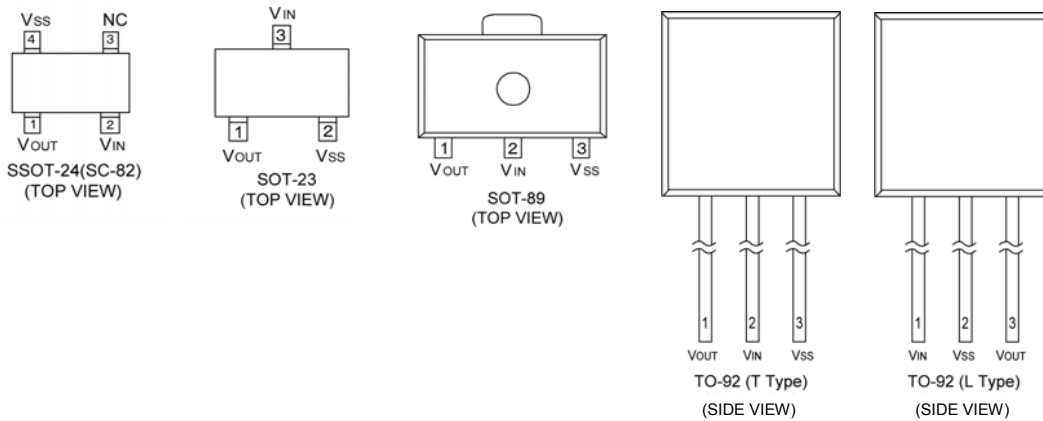


N-ch Open Drain Output

TYPICAL PERFORMANCE CHARACTERISTICS



PIN CONFIGURATION



PIN ASSIGNMENT

| PIN NUMBER | | | | | PIN NAME | FUNCTION |
|------------|--------|--------|-----------|-----------|------------------|----------------|
| SSOT-24 | SOT-23 | SOT-89 | TO-92 (T) | TO-92 (L) | | |
| 2 | 3 | 2 | 2 | 1 | V _{IN} | Supply Voltage |
| 4 | 2 | 3 | 3 | 2 | V _{SS} | Ground |
| 1 | 1 | 1 | 1 | 3 | V _{OUT} | Output |
| 3 | - | - | - | - | NC | No Connection |

PRODUCT CLASSIFICATION

Ordering Information

XC61C①②③④⑤⑥⑦⑧^(*)

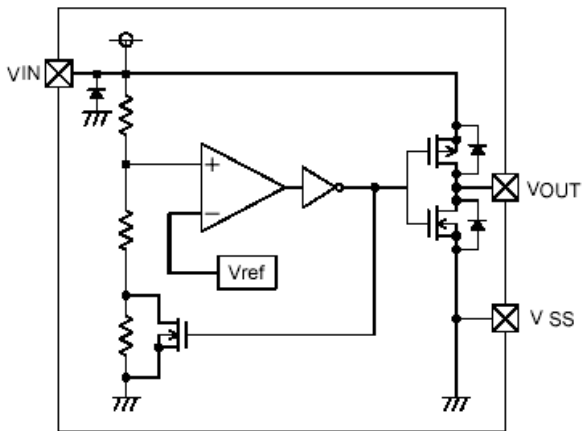
| DESIGNATOR | DESCRIPTION | SYMBOL | DESCRIPTION |
|------------|--------------------------------------|---------|---|
| ① | Output Configuration | C | CMOS output |
| | | N | N-ch open drain output |
| ② ③ | Detect Voltage | 08 ~ 60 | e.g.0.9V → ②0, ③9 |
| | | | e.g.1.5V → ②1, ③5 |
| ④ | Output Delay | 0 | No delay |
| ⑤ | Detect Accuracy | 1 | Within ±1% (V _{DF(T)} =2.6V~5.0V) |
| | | 2 | Within ±2% |
| ⑥⑦⑧ | Packages Taping Type ^(**) | NR | SSOT-24 (SC-82) |
| | | NR-G | SSOT-24 (SC-82) (Halogen & Antimony free) |
| | | MR | SOT-23 |
| | | MR-G | SOT-23 (Halogen & Antimony free) |
| | | PR | SOT-89 |
| | | PR-G | SOT-89 (Halogen & Antimony free) |
| | | TH | TO-92 (Standard) Taping Type: Paper type |
| | | TB | TO-92 (Standard) Taping Type: Bag |
| | | LH | TO-92 (Custom pin configuration) Taping Type: Paper type (Discontinued Product) |
| | | LB | TO-92 (Custom pin configuration) Taping Type: Bag (Discontinued Product) |

^(*) The “-G” suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.

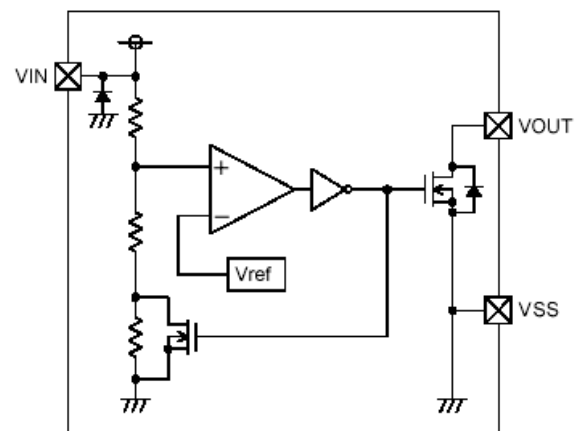
^(**) The device orientation is fixed in its embossed tape pocket. For reverse orientation, please contact your local Torex sales office or representative. (Standard orientation: ⑥R-⑧, Reverse orientation: ⑥L-⑧)

■ BLOCK DIAGRAMS

(1) CMOS Output



(2) N-ch Open Drain Output



■ ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|-----------------------------|---------------------------|--------|-----------------------|-------|
| Input Voltage | *1 | VIN | 9.0 | V |
| | *2 | | 12.0 | |
| Output Current | | IOUT | 50 | mA |
| Output Voltage | CMOS | VOUT | VSS - 0.3 ~ VIN + 0.3 | V |
| | N-ch Open Drain Output *1 | | VSS - 0.3 ~ 9.0 | |
| | N-ch Open Drain Output *2 | | VSS - 0.3 ~ 12.0 | |
| Power Dissipation | SSOT-24 | Pd | 150 | mW |
| | SOT-23 | | 150 | |
| | SOT-89 | | 500 | |
| | TO-92 | | 300 | |
| Operating Temperature Range | | Topr | -40 ~ +85 | °C |
| Storage Temperature Range | | Tstg | -40 ~ +125 | °C |

*1: Low voltage: VDF(T)=0.8V~1.5V

*2: Standard voltage: VDF(T)=1.6V~6.0V

ELECTRICAL CHARACTERISTICS

V_{DF(T)} = 0.8V to 6.0V ± 2%

V_{DF(T)} = 2.6V to 5.0V ± 1%

T_a=25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUITS | |
|---|---|--|---|---------------------------|------------------------------|--------|----------|----|
| Detect Voltage | V _{DF} | V _{DF(T)} =0.8V~1.5V *1 V _{DF(T)} =1.6V~6.0V *2 | V _{DF(T)} x 0.98 | V _{DF(T)} | V _{DF(T)} x 1.02 | V | 1 | |
| | | V _{DF(T)} =2.6V~5.0V *2 | V _{DF(T)} x 0.99 | V _{DF(T)} | V _{DF(T)} x 1.01 | V | 1 | |
| Hysteresis Range | V _{HYS} | | V _{DF} x 0.02 | V _{DF} x 0.05 | V _{DF} x 0.08 | V | 1 | |
| Supply Current | I _{SS} | V _{IN} = 1.5V | - | 0.7 | 2.3 | μA | 2 | |
| | | V _{IN} = 2.0V | - | 0.8 | 2.7 | | | |
| | | V _{IN} = 3.0V | - | 0.9 | 3.0 | | | |
| | | V _{IN} = 4.0V | - | 1.0 | 3.2 | | | |
| | | V _{IN} = 5.0V | - | 1.1 | 3.6 | | | |
| Operating Voltage *1 | V _{IN} | V _{DF(T)} = 0.8V to 1.5V | 0.7 | - | 6.0 | V | 1 | |
| Operating Voltage *2 | | V _{DF(T)} = 1.6V to 6.0V | 0.7 | - | 10.0 | | | |
| Output Current *1 | I _{OUT} | N-ch V _{Ds} = 0.5V | V _{IN} = 0.7V | 0.10 | 0.80 | - | mA | 3 |
| | | | V _{IN} = 1.0V | 0.85 | 2.70 | - | | |
| CMOS, P-ch V _{Ds} = 2.1V | | V _{IN} = 6.0V | - | -7.5 | -1.5 | 4 | | |
| | | V _{IN} = 1.0V | 1.0 | 2.2 | - | | | |
| Output Current *2 | | N-ch V _{Ds} = 0.5V | V _{IN} = 2.0V | 3.0 | 7.7 | - | | 3 |
| | | | V _{IN} = 3.0V | 5.0 | 10.1 | - | | |
| | | | V _{IN} = 4.0V | 6.0 | 11.5 | - | | |
| | | | V _{IN} = 5.0V | 7.0 | 13.0 | - | | |
| | | | CMOS, P-ch V _{Ds} = 2.1V | V _{IN} = 8.0V | - | -10.0 | | |
| Leak Current | | I _{leak} | V _{IN} =6.0V, V _{OUT} =6.0V*1 | CMOS | | - | | nA |
| | V _{IN} =10.0V, V _{OUT} =10.0V*2 | | N-ch Open Drain | | - | 100 | | |
| Temperature Characteristics | $\frac{\Delta V_{DF}}{\Delta T_{opr} \cdot V_{DF}}$ | -40°C ≤ T _{opr} ≤ 85°C | - | ±100 | - | ppm/°C | - | |
| Delay Time (V _{DR} →V _{OUT} inversion) | t _{DLY} | Inverts from V _{DR} to V _{OUT} | - | 0.03 | 0.20 | ms | 5 | |

NOTE:

*1: Low Voltage: V_{DF(T)}=0.8V~1.5V

*2: Standard Voltage: V_{DF(T)}=1.6V~6.0V

V_{DF(T)}: Setting detect voltage

Release Voltage: V_{DR} = V_{DF} + V_{HYS}

OPERATIONAL EXPLANATION

(Especially prepared for CMOS output products)

- ① When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN} .
(A condition of high impedance exists with N-ch open drain output configurations.)
- ② When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.
- ③ When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pulled-up.)
- ④ When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.
- ⑤ When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN} .
(A condition of high impedance exists with N-ch open drain output configurations.)
- ⑥ The difference between V_{DR} and V_{DF} represents the hysteresis range.

Timing Chart



NOTES ON USE

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current (I_{OUT}) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (I_{OUT}) does not exist. (refer to the Oscillation Description (2) below)
4. With a resistor connected between the V_{IN} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN} pin.
5. In order to stabilize the IC's operations, please ensure that V_{IN} pin's input frequency's rise and fall times are more than several μ sec / V.
6. Please use N-ch open drains configuration, when a resistor R_{IN} is connected between the V_{IN} pin and power source. In such cases, please ensure that R_{IN} is less than $10k\Omega$ and that C is more than $0.1\mu F$.

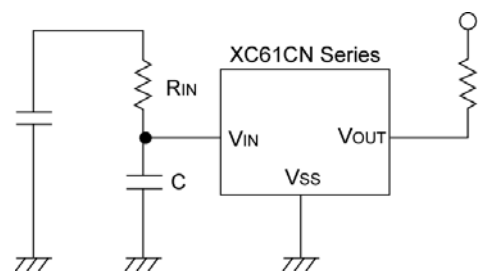


Figure 1: Circuit using an input resistor

Oscillation Description

(1) Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (I_{OUT}) will flow at R_L . Because a voltage drop ($R_{IN} \times I_{OUT}$) is produced at the R_{IN} resistor, located between the input (IN) and the V_{IN} pin, the load current will flow via the IC's V_{IN} pin. The voltage drop will also lead to a fall in the voltage level at the V_{IN} pin. When the V_{IN} pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at R_{IN} will disappear, the voltage level at the V_{IN} pin will rise and release operations will begin over again.

Oscillation may occur with this " release - detect - release " repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the XC61C series are CMOS IC s, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations. (refer to Figure 3)

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

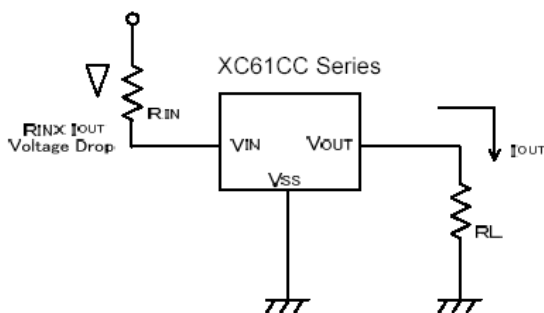


Figure 2: Oscillation in relation to output current

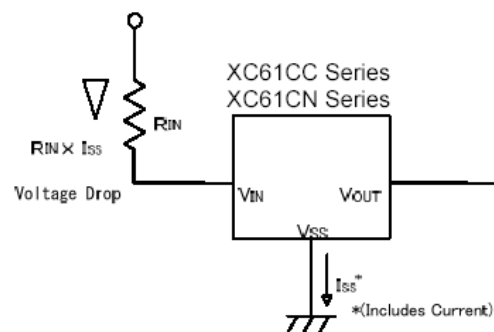


Figure 3: Oscillation in relation to through current

■ TEST CIRCUITS

Circuit 1



Circuit 2



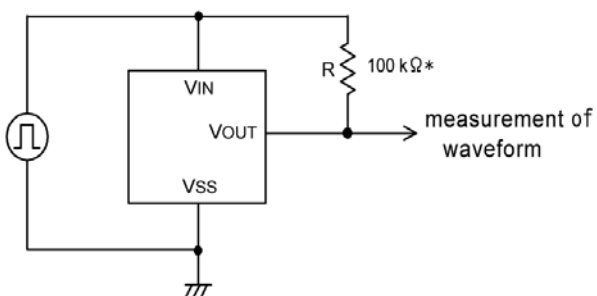
Circuit 3



Circuit 4



Circuit 5



* : A resistor is not necessary with CMOS output products.

TYPICAL PERFORMANCE CHARACTERISTICS

Low Voltage

(1) Supply Current vs. Input Voltage



(2) Detect, Release Voltage vs. Ambient Temperature



(3) Output Voltage vs. Input Voltage

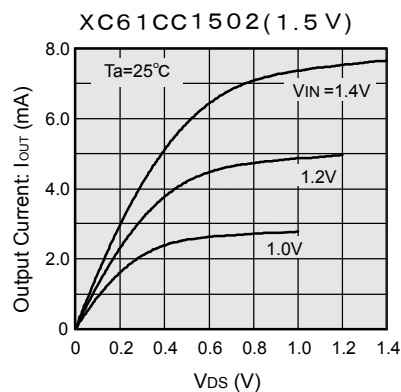
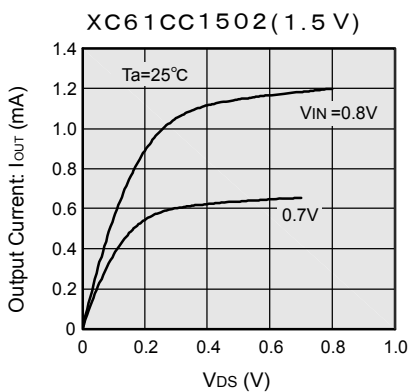
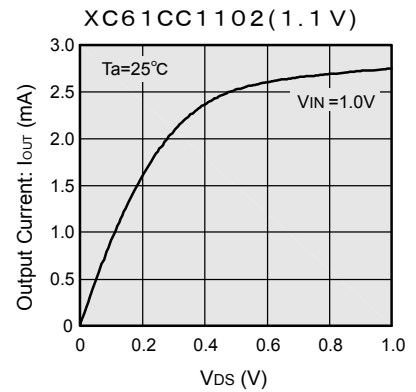
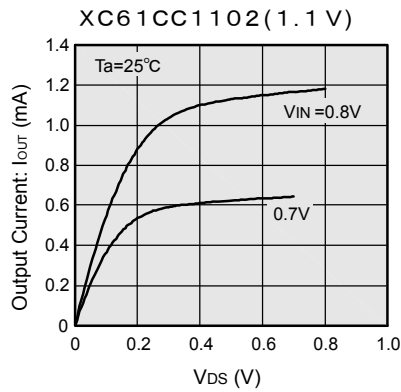
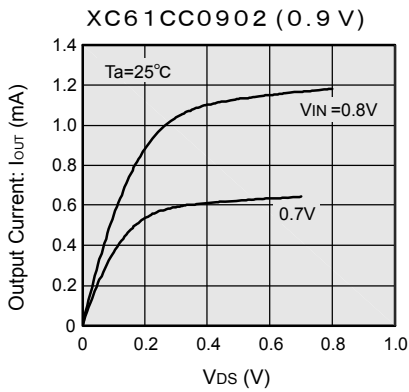


Note : Unless otherwise stated, the N-channel open drain pull-up resistance value is 100kΩ.

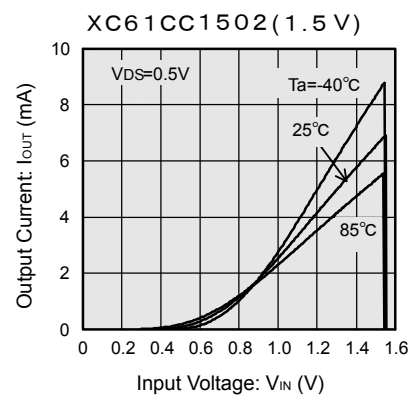
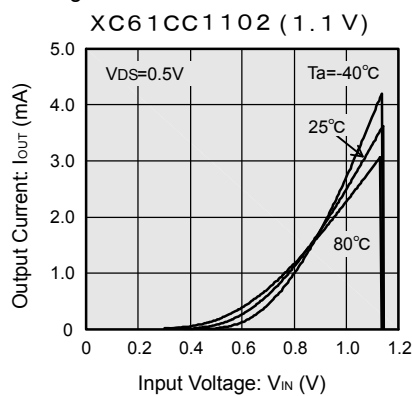
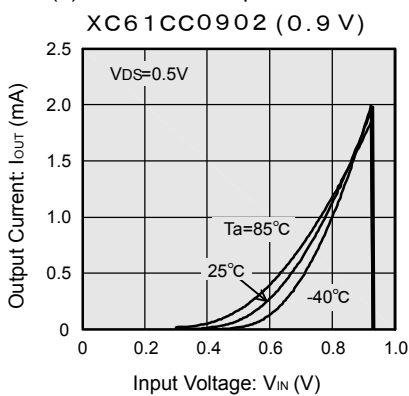
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

● Low Voltage (Continued)

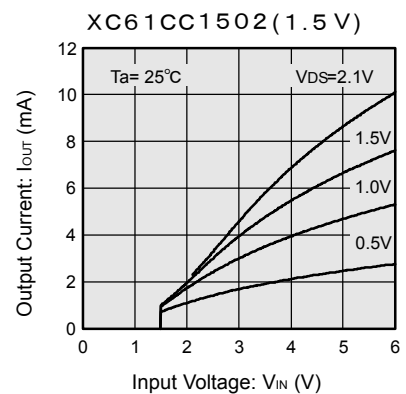
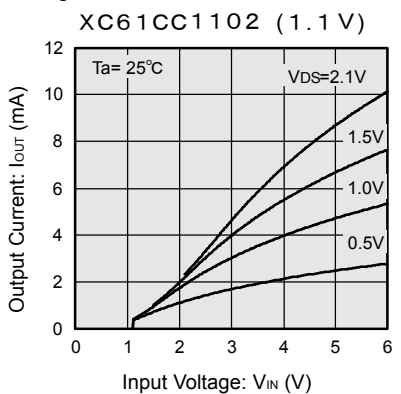
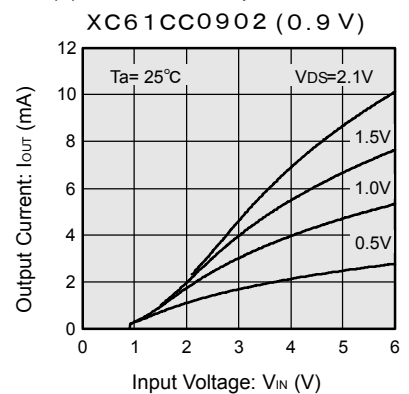
(4) N-ch Driver Output Current vs. V_{DS}



(5) N-ch Driver Output Current vs. Input Voltage



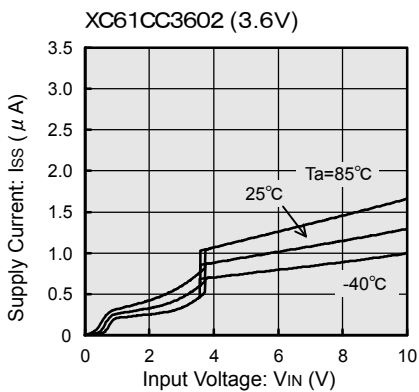
(6) P-ch Driver Output Current vs. Input Voltage



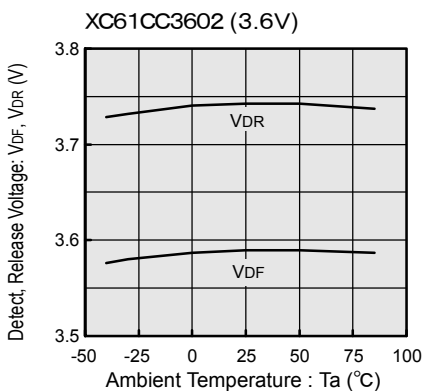
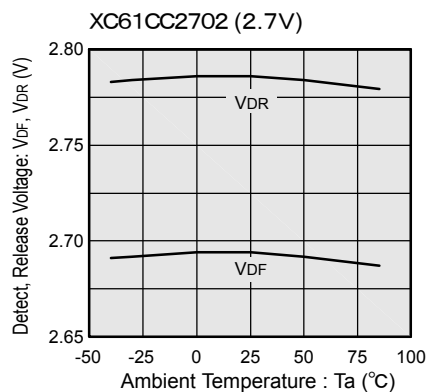
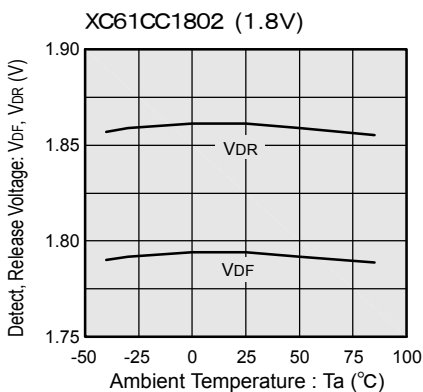
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Standard Voltage

(1) Supply Current vs. Input Voltage



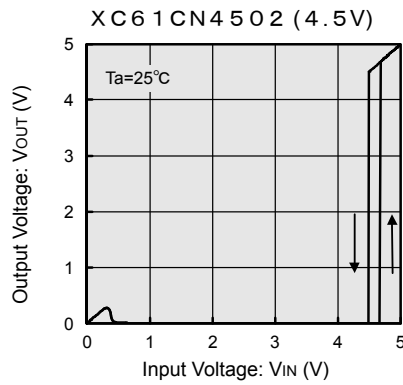
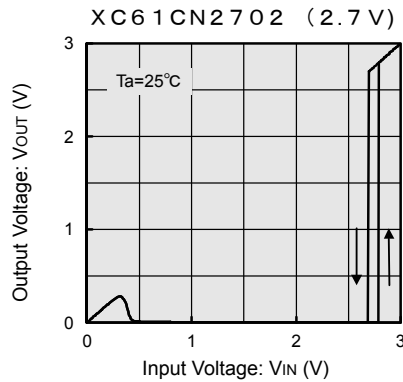
(2) Detect, Release Voltage vs. Ambient Temperature



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

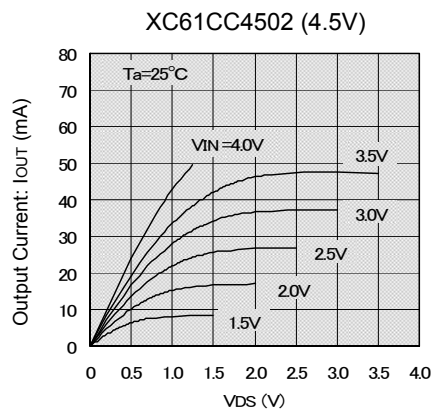
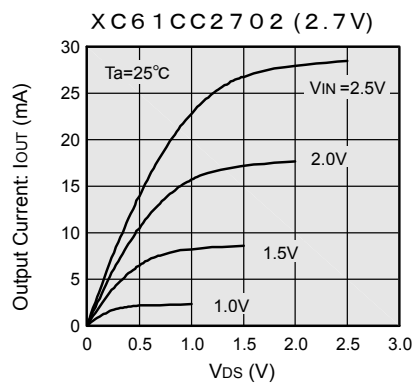
● Standard Voltage (Continued)

(3) Output Voltage vs. Input Voltage



Note : The N-channel open drain pull up resistance value is 100kΩ.

(4) N-ch Driver Output Current vs. V_{DS}



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

● Standard Voltage (Continued)

(4) N-ch Driver Output Current vs. V_{DS}



(5) N-ch Driver Output Current vs. Input Voltage



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

● Standard Voltage (Continued)

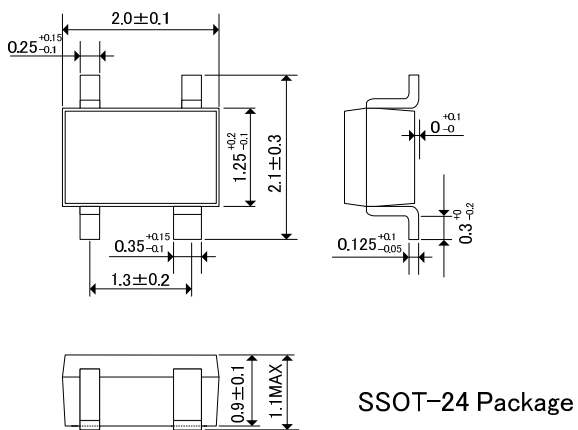
(6) P-ch Driver Output Current vs. Input Voltage



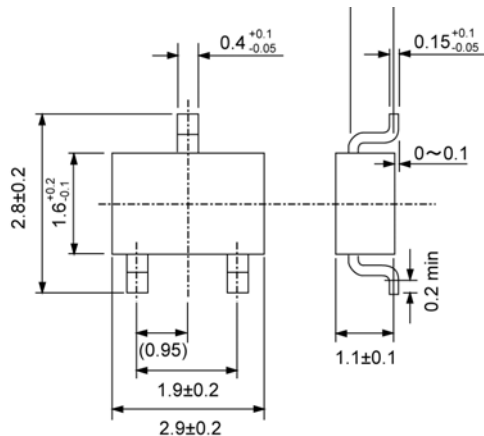
PACKAGING INFORMATION

● SSOT-24 (SC-82)

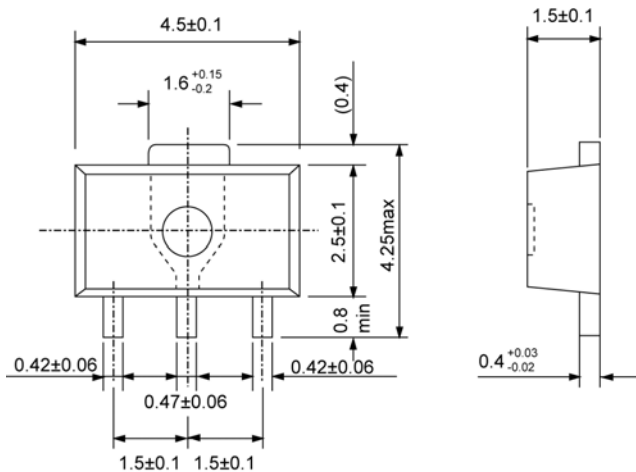
(unit : mm)



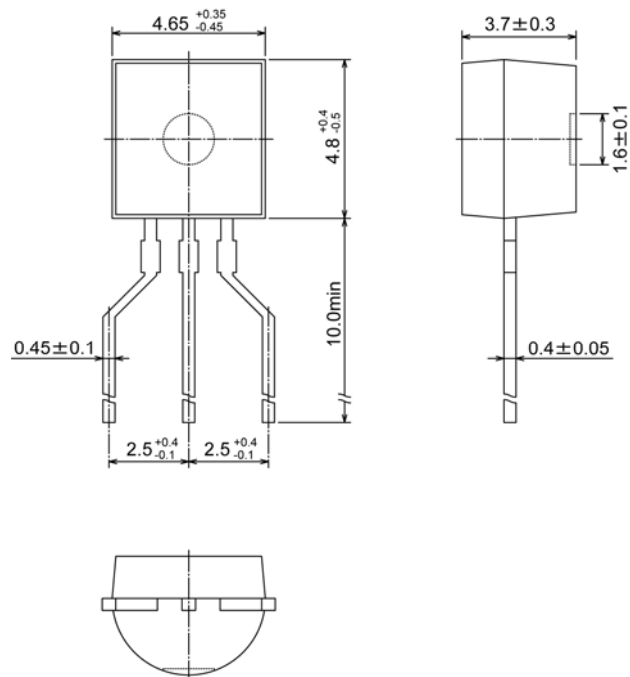
● SOT-23



● SOT-89



● TO-92



MARKING RULE

- SSOT-24, SOT-23, SOT-89



- ① represents integer of detect voltage and CMOS Output (XC61CC series)

| MARK | CONFIGURATION | VOLTAGE (V) |
|------|---------------|-------------|
| A | CMOS | 0.X |
| B | CMOS | 1.X |
| C | CMOS | 2.X |
| D | CMOS | 3.X |
| E | CMOS | 4.X |
| F | CMOS | 5.X |
| H | CMOS | 6.X |

- N-Channel Open Drain Output (XC61CN series)

| MARK | CONFIGURATION | VOLTAGE (V) |
|------|---------------|-------------|
| K | N-ch | 0.X |
| L | N-ch | 1.X |
| M | N-ch | 2.X |
| N | N-ch | 3.X |
| P | N-ch | 4.X |
| R | N-ch | 5.X |
| S | N-ch | 6.X |

- ② represents decimal number of detect voltage

| MARK | VOLTAGE (V) | MARK | VOLTAGE (V) |
|------|-------------|------|-------------|
| 0 | X.0 | 5 | X.5 |
| 1 | X.1 | 6 | X.6 |
| 2 | X.2 | 7 | X.7 |
| 3 | X.3 | 8 | X.8 |
| 4 | X.4 | 9 | X.9 |

- ③ represents delay time
(Except for SSOT-24)

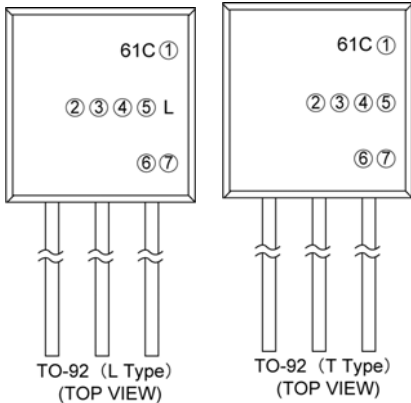
| MARK | DELAY TIME | PRODUCT SERIES |
|------|---------------|----------------|
| 3 | No Delay Time | XC61Cxxx0xxx |

- ④ represents production lot number

Based on the internal standard. (G, I, J, O, Q, W excluded)

MARKING RULE (Continued)

TO-92



① represents output configuration

| MARK | OUTPUT CONFIGURATION |
|------|----------------------|
| C | CMOS |
| N | N-ch |

②, ③ represents detect voltage (ex.)

| MARK | | VOLTAGE (V) |
|------|---|-------------|
| ② | ③ | |
| 3 | 3 | 3.3 |
| 5 | 0 | 5.0 |

④ represents delay time

| MARK | DELAY TIME |
|------|------------|
| 0 | No delay |

⑤ represents detect voltage accuracy

| MARK | DETECT VOLTAGE ACCURACY |
|------|--------------------------------|
| 1 | Within $\pm 1\%$ (Semi-custom) |
| 2 | Within $\pm 2\%$ |

⑥ represents a least significant digit of production year

| MARK | PRODUCTION YEAR |
|------|-----------------|
| 5 | 2005 |
| 6 | 2006 |

⑦ represents production lot number

0 to 9, A to Z repeated. (G, I, J, O, Q, W excluded)

* No character inversion used.

1. The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.
2. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.
3. Please ensure suitable shipping controls (including fail-safe designs and aging protection) are in force for equipment employing products listed in this datasheet.
4. The products in this datasheet are not developed, designed, or approved for use with such equipment whose failure or malfunction can be reasonably expected to directly endanger the life of, or cause significant injury to, the user.
(e.g. Atomic energy; aerospace; transport; combustion and associated safety equipment thereof.)
5. Please use the products listed in this datasheet within the specified ranges.
Should you wish to use the products under conditions exceeding the specifications, please consult us or our representatives.
6. We assume no responsibility for damage or loss due to abnormal use.
7. All rights reserved. No part of this datasheet may be copied or reproduced without the prior permission of TOREX SEMICONDUCTOR LTD.

TOREX SEMICONDUCTOR LTD.