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## PIC12F629/675 Rev. A Silicon/Data Sheet Errata

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The PIC12F629/675 parts you have received conform functionally to the Device Data Sheet (DS41190C), except for the anomalies described below.

All issues listed here will be addressed in future revisions of the **PIC12F629/675 silicon**.

### 1. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

#### **Work around**

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer interrupt service routine to verify the EEPROM write success.
4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

### Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41190C), the following clarifications and corrections should be noted.

### 1. Module: GPIO Port

Register 3-2, "TRISIO – GPIO Tri-state Register (Address: 85h)", is incorrect. Bits 5-4 and 2-0 should read "R/W-1", as shown below:

# PIC12F629/675

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## REGISTER 3-2: TRISIO – GPIO TRI-STATE REGISTER (ADDRESS: 85h)

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1	
—	—	TRISIO5	TRISIO4	TRISIO3 <sup>(1)</sup>	TRISIO2	TRISIO1	TRISIO0	
bit 7								bit 0

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **TRISIO<5:0>**: General Purpose I/O Tri-State Control bit  
1 = GPIO pin configured as an input (tri-stated)  
0 = GPIO pin configured as an output

**Note 1:** TRISIO<3> always reads '1'.

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

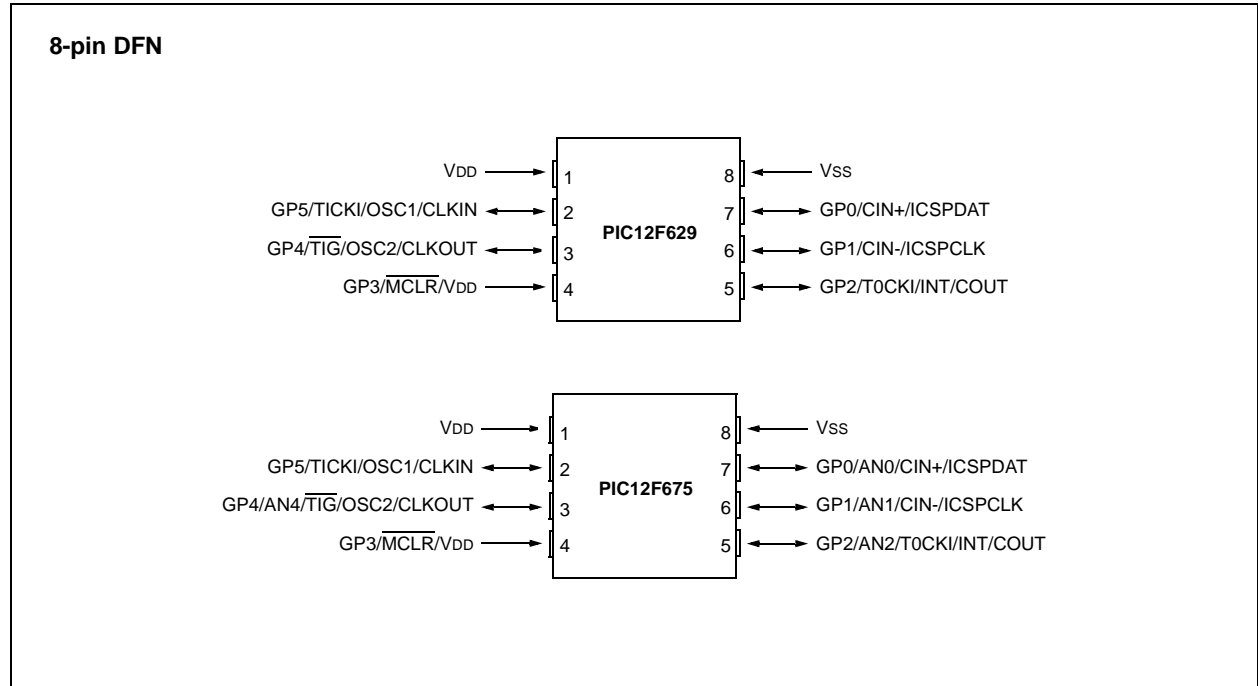
'0' = Bit is cleared

x = Bit is unknown

## 2. Module: New 4x4 DFN Package Added

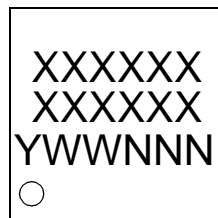
The new 8-pin 4x4 DFN pinout diagram will be added to the Pin Diagrams figure on page 2 and the Packaging Information chapter as shown below:

### Pin Diagrams

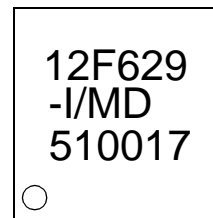


## 14.1 Package Marking Information

8-Lead DFN

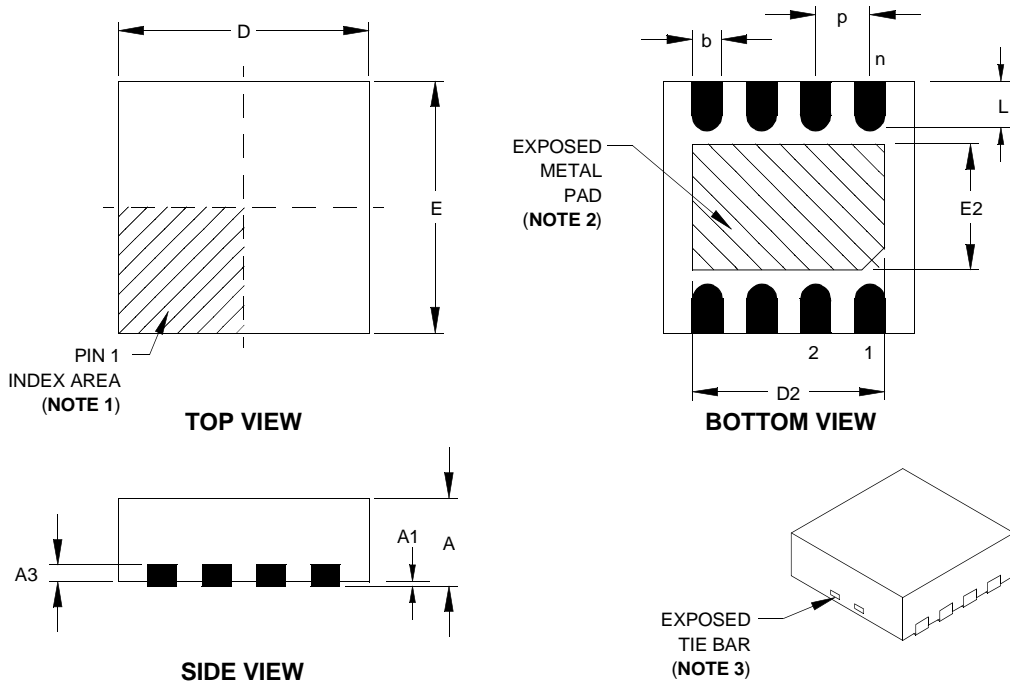


Example



# PIC12F629/675

## 8-Lead Plastic Dual Flat No Lead Package (MD) 4x4x0.9 mm Body (DFN) – Saw Singulated



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	P	.031 BSC			0.80 BSC		
Overall Height	A	.029	.035	.039	0.75	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3	.008 REF.			0.20 REF.		
Overall Length	E	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Width (Note 3)	E2	.091	.106	.112	2.30	2.70	2.85
Overall Width	D	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Length (Note 3)	D2	.127	.138	.144	3.23	3.50	3.65
Contact Width	b	.009	.012	.015	0.23	0.30	0.38
Contact Length	§	L	.008	.016	.020	0.40	0.50
Contact-to-Exposed Pad	§	K	.008	-	0.20	-	-

\* Controlling Parameter

§ Significant Characteristic

### Notes:

- Package may have one or more exposed tie bars at ends.
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Exposed pad dimensions vary with paddle size.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

JEDEC equivalent: Not Registered

Drawing No. C04-131

Revised 9-14-05

## APPENDIX A: REVISION HISTORY

### Rev. A Document (3/2002)

First revision of this document. Revised Table 12.3

### Rev. B Document (9/2002)

Added Module 1: "In-Circuit Serial Programming™", changes made to the Typical In-Circuit Serial Programming Connection, Figure 9-18.

### Rev. C Document (04/02/04)

Removed Table 12.3 and Figure 9-18 due to Data Sheet revisions.

Added Module 1: "GPIO Port", changes made to the TRISIO – GPIO Tri-state Register.

### Rev. D Document (11/2004)

Added Module 1: "Data EEPROM Memory" for PIC12F629/675 silicon.

### Rev. E Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 2: New 4x4 DFN Package added.

### Rev. F Document (10/2005)

Data Sheet Clarifications/Corrections Section: Replaced 8-Lead Plastic Dual Flat No Lead Package 4x4 (DFN).

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NOTES:

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