FAIRCHILD SEMICONDUCTOR®

March 1995
Revised February 2005

74LCX125
Low Voltage Quad Buffer with 5V Tolerant Inputs and Outputs

General Description

The LCX125 contains four independent non-inverting buffers with 3-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX125 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.0 ns t_{PD} max (V_{CC} = 3.3V), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
  Human body model > 2000V
  Machine model > 100V
- Leadless Pb-Free DQFN package

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX125MX_NL (Note 3)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX125SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX125BQX (Note 2)	MLP014A	Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74LCX125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX125MTCX_NL (Note 3)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 2: DQFN package available in Tape and Reel only.

Note 3: "_NL" indicates Pb-Free package (per JEDED J-STD-020B). Device available in Tape and Reel only.

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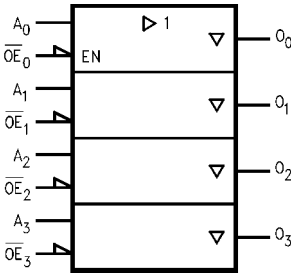
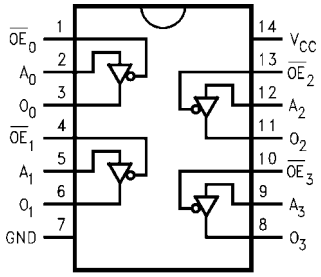
Logic Symbol

IEEE/IEC



Connection Diagrams

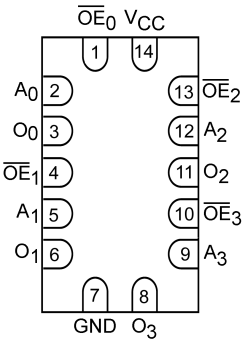
Pin Assignments for SOIC, SOP, and TSSOP



Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{OE}_n$	Output Enable Inputs
O_n	Outputs

Pad Assignments for DQFN



(Top View)

Truth Table

Inputs		Output
$\overline{OE}_n$	A_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

Absolute Maximum Ratings(Note 4)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 5)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 6)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24.0	mA
		V_{CC} = 2.7V – 3.0V		±12.0	
		V_{CC} = 2.3V – 2.7V		±8.0	
T_A	Free-Air Operating Temperature		−40.0	85.0	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10.0	ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Unused inputs or I/Os must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.3 – 3.6	V_{CC} – 0.2		V
		I_{OH} = -8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 – 3.6		0.2	V
		I_{OL} = 8mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		10.0	μA
		$3.6V \le V_I$, $V_O \le 5.5V$ (Note 7)	2.3 – 3.6		±10.0	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	6.0	1.5	6.5	1.5	7.2	ns
t_{PLH}		1.5	6.0	1.5	6.5	1.5	7.2	
t_{PZL}	Output Enable Time	1.5	7.0	1.5	8.0	1.5	9.1	ns
t_{PZH}		1.5	7.0	1.5	8.0	1.5	9.1	
t_{PLZ}	Output Disable Time	1.5	6.0	1.5	7.0	1.5	7.2	ns
t_{PHZ}		1.5	6.0	1.5	7.0	1.5	7.2	
t_{OSHL}	Output to Output Skew (Note 8)		1.0					ns
t_{OSLH}			1.0					

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	25.0	pF

AC Loading and Waveforms Generic for LCX Family

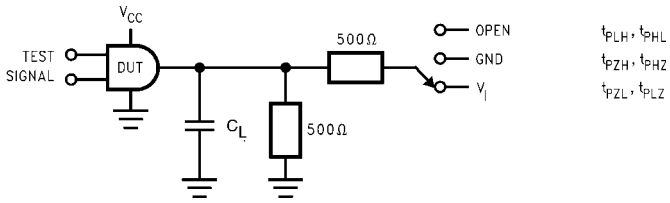
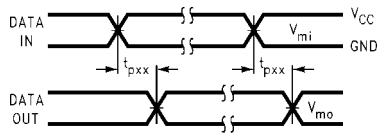
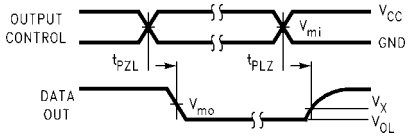


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

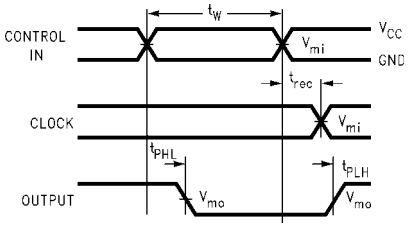
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH},t_{PHZ}	GND



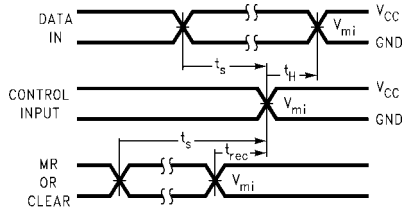
Waveform for Inverting and Non-Inverting Functions



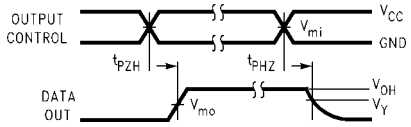
3-STATE Output Low Enable and Disable Times for Logic



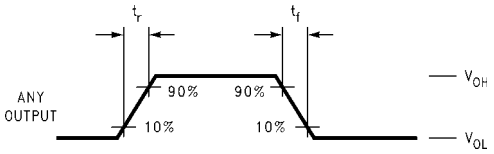
Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold TIme and Recovery TIme for Logic



3-STATE Output High Enable and Disable TImes for Logic

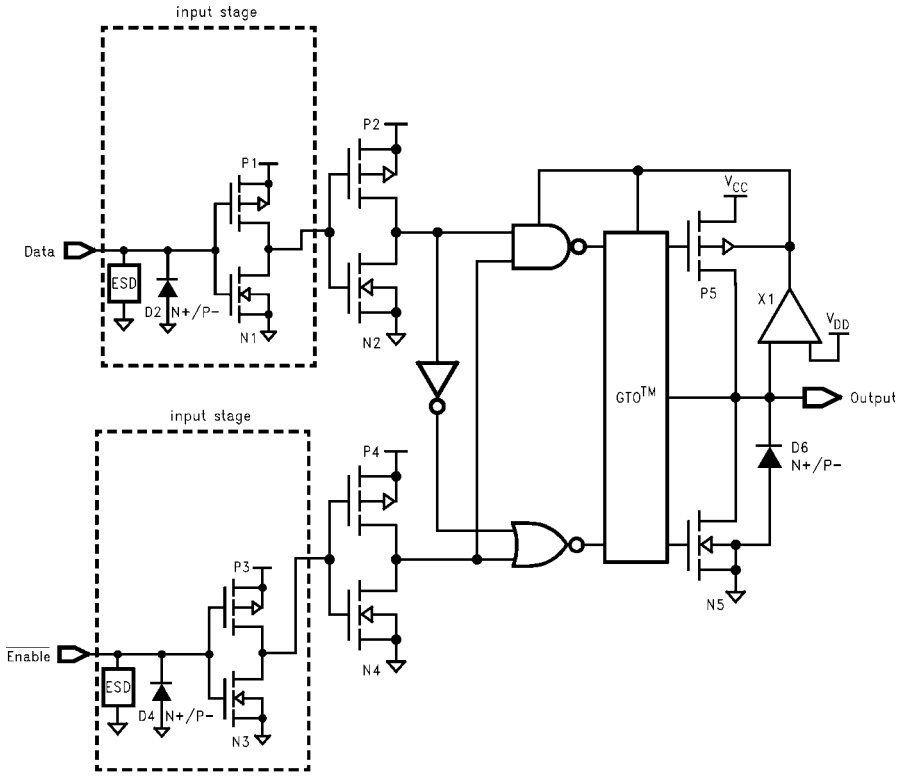


t_{rise} and t_{fall}

FIGURE 2. Waveforms
(Input Pulse Characteristics; f = 1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family

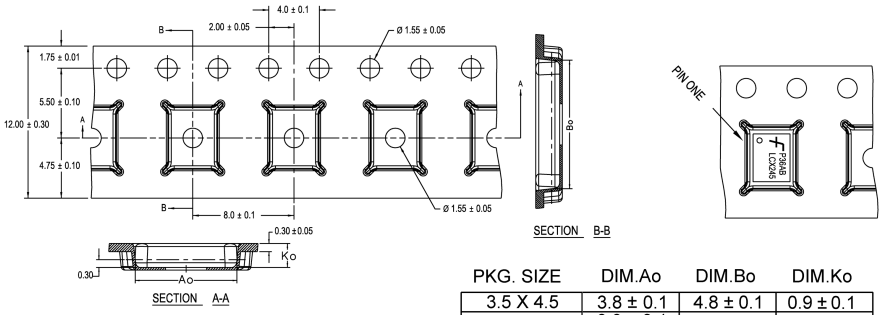


Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



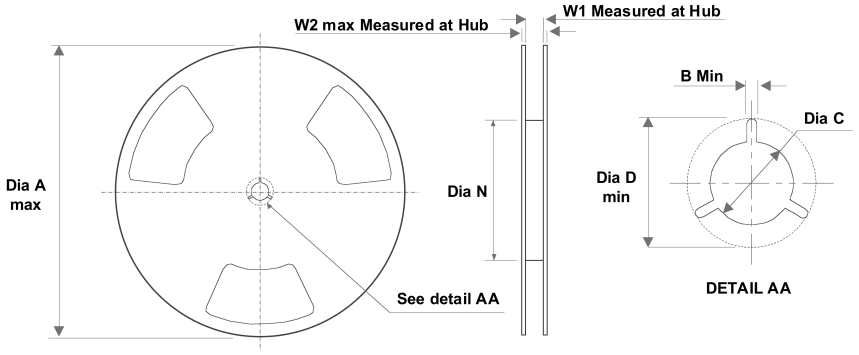
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

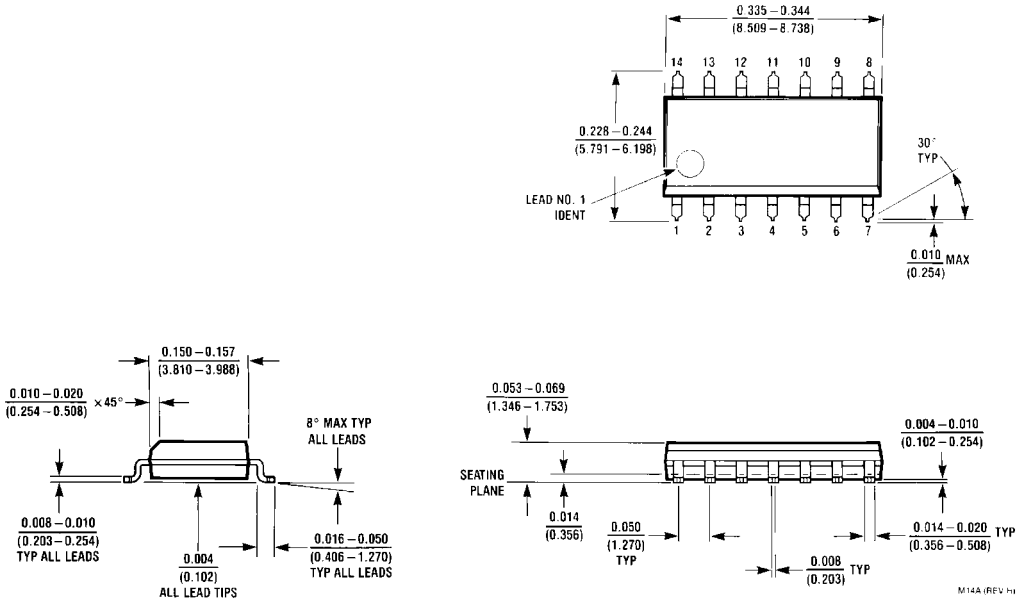
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

REEL DIMENSIONS inches (millimeters)



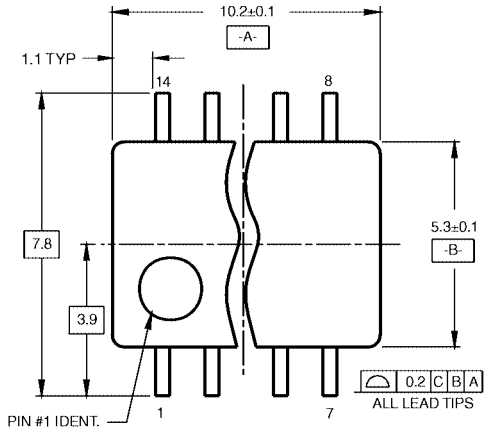
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

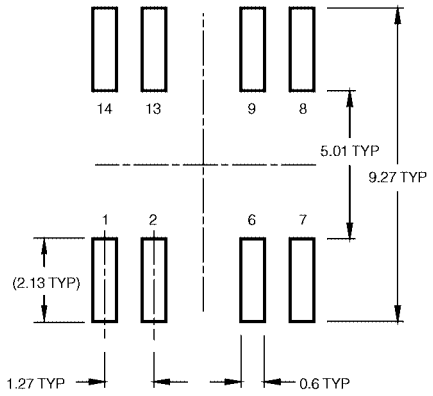
Physical Dimensions inches (millimeters) unless otherwise noted



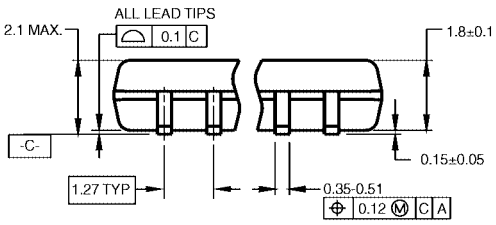
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

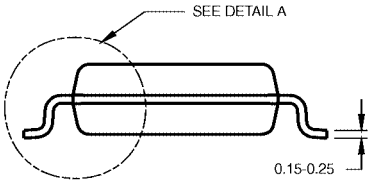
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



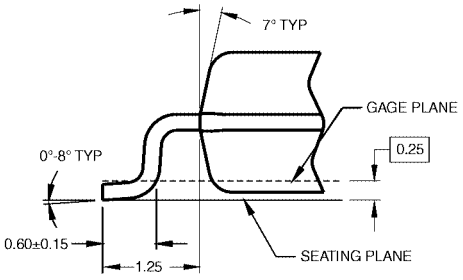


LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

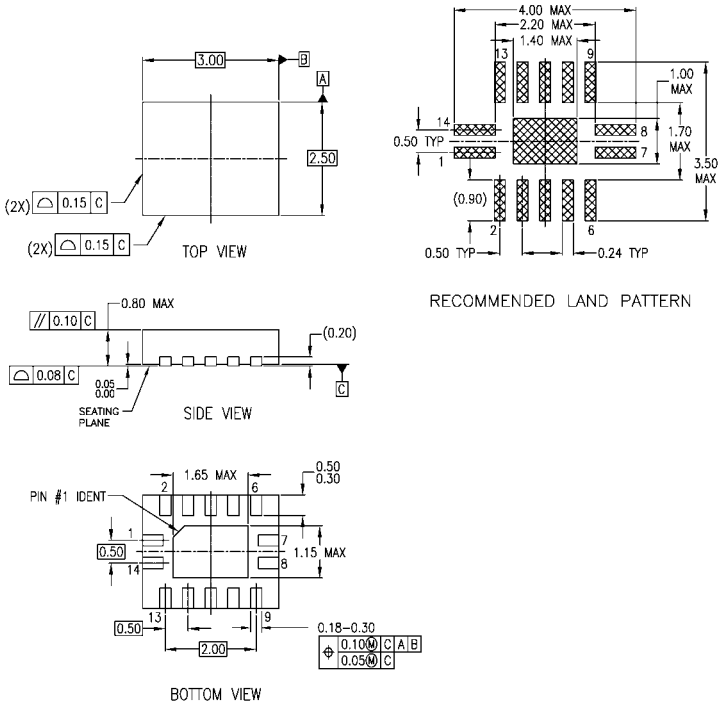
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



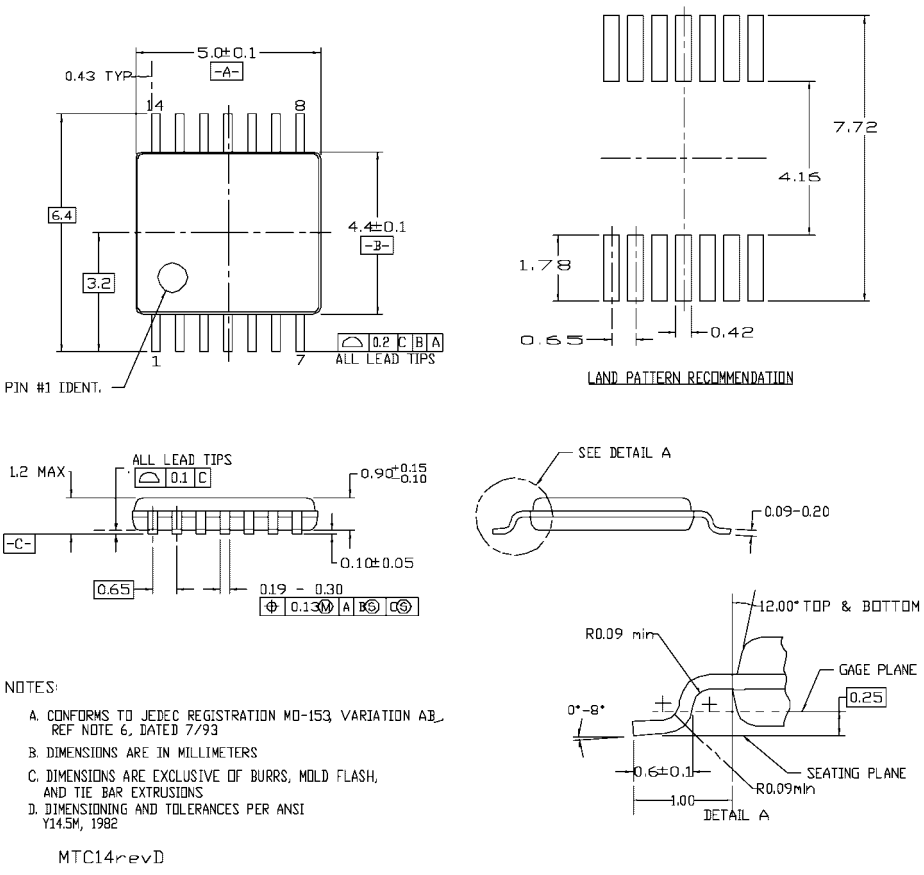
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AA
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP014ArevA

Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
Package Number MLP014A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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