Specification Sheet

Model No. : HSM320240C

Description : 320*240 STN LCD Module ,Backlight Color Option , AIP31066 Controller,Wide Temp, Popular Size.

RECORDS OF REVISION

Date	Rev.	Description	Page	Design by
2012/12/23	0	New Sample.	-	-
			-	-

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1. SPECIFICATIONS

1.1 Features

Item	Standard Value
Display Type	320 x 240 DOTS
Driver Condition	LCD Module : 1/240 Duty , 1/17 Bias
Viewing Direction	6 O'Clock
Interface	8BIT bus MPU interface
Driver IC	RA8835 or eqv

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	139(L) *100(W) * 12.5 (T)	mm
Viewing Area	103(L) * 79(W)	mm
Dot Size (W*H)	0.27*0.27mm	
Dot Pitch (W*H)	0.30*0.30 mm	

HSM320240C Series Table

No.	Part Number	LCD Type	Backlight Color	Graphic & Font Color	Background Color
1	HSM320240C-B	STN,Blue,Negative, Transmissive	White	White	Blue
2	HSM320240C-Y	STN,Yellow-Green, Positive, Transflective	Yellow-Green	Black	Yellow-Green
3	HSM320240C-G	STN,Gray,Positive, Transflective	White	Dark-Blue	Gray
4	HSM320240C-G-W	FSTN,Gray,Positive, Transflective	White	Black	Gray
5	HSM320240C-G-O	FSTN,Gray,Positive, Transflective	Orange	Black	Orange
6	HSM320240C-G-R	FSTN,Gray,Positive, Transflective	Red	Black	Red

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
System Power Supply Voltage	VDD	-	-0.3	5.5	V
LCD Driver Supply Voltage	$VOUT_{IN}$	-	4.8	5.0	V
Input Voltage	V_{IN}	-	-0.3	VDD + 0.2	V
Operating Temperature	T_{OP}	-	-20	70	°C
Storage Temperature	T_{ST}	-	-30	80	°C
Storage Humidity	H_D	Ta < 40 °C	20	80	%RH

1.4 Backlight Characteristics

LCD Module with LED Backlight

Electrical / Optical Characteristics

Ta =25℃

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	Vf	If=160mA	3.0	3.1	3.2	V
Reverse Current	Ir	If=5v			--	uA
Average Brightness	IV	If=160mA				cd/m^2
Wavelength (Without LCD)	λ d	If=160mA	--	--	--	nm
Luminous Intensity (without LCD)	Lv Sub	If=160mA				cd/m^2
Uniformity	Δ%	IvMin / IvMax *100%	--	-	-	%
Color	WHITE					

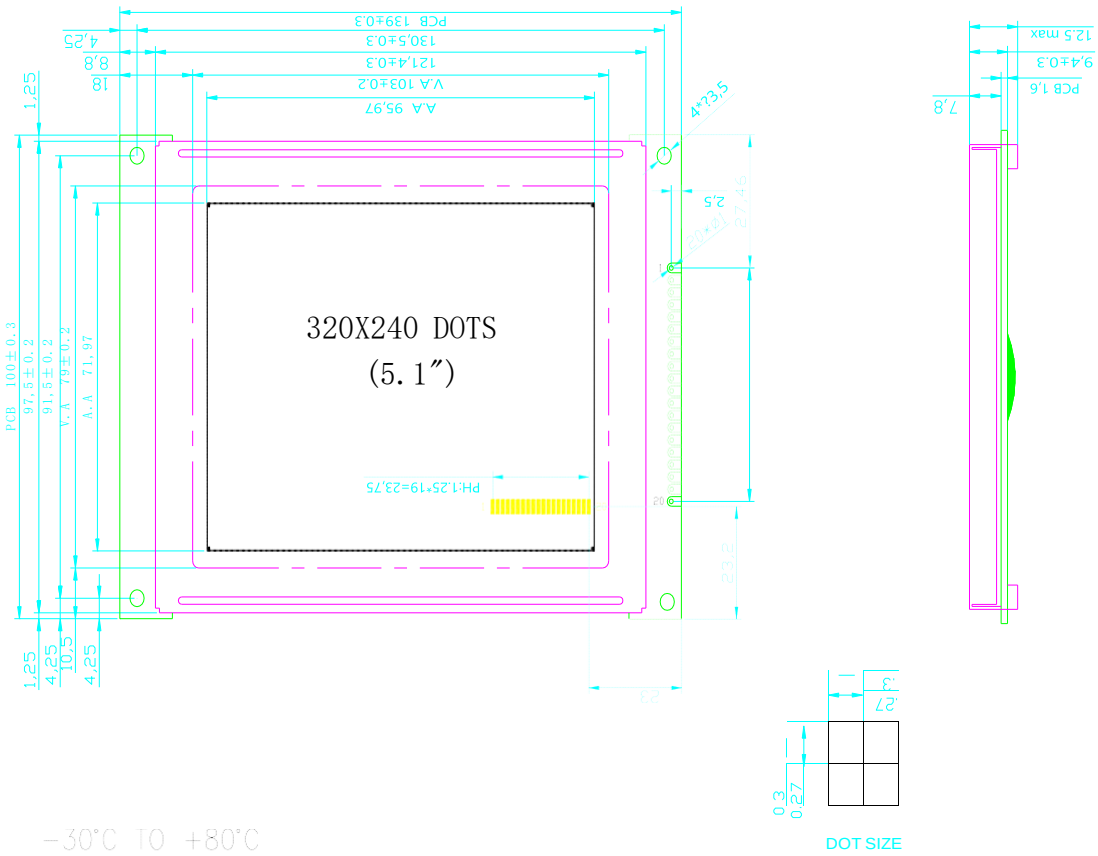
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

INTERFACE:	
1	VSS
2	VCC(5V)
3	V0
4	/WR
5	/RD
6	/CS
7	A0
8	/RST
9	DB0
10	DB1
11	DB2
12	DB3
13	DB4
14	DB5
15	DB6
16	DB7
17	LEDA
18	VEE
19	LEDA
20	LEDK

VER	DETIAL DISCRIPTION	DATE
00	FIRST ISSUE	2012-11-10



SPECIFICATIONS

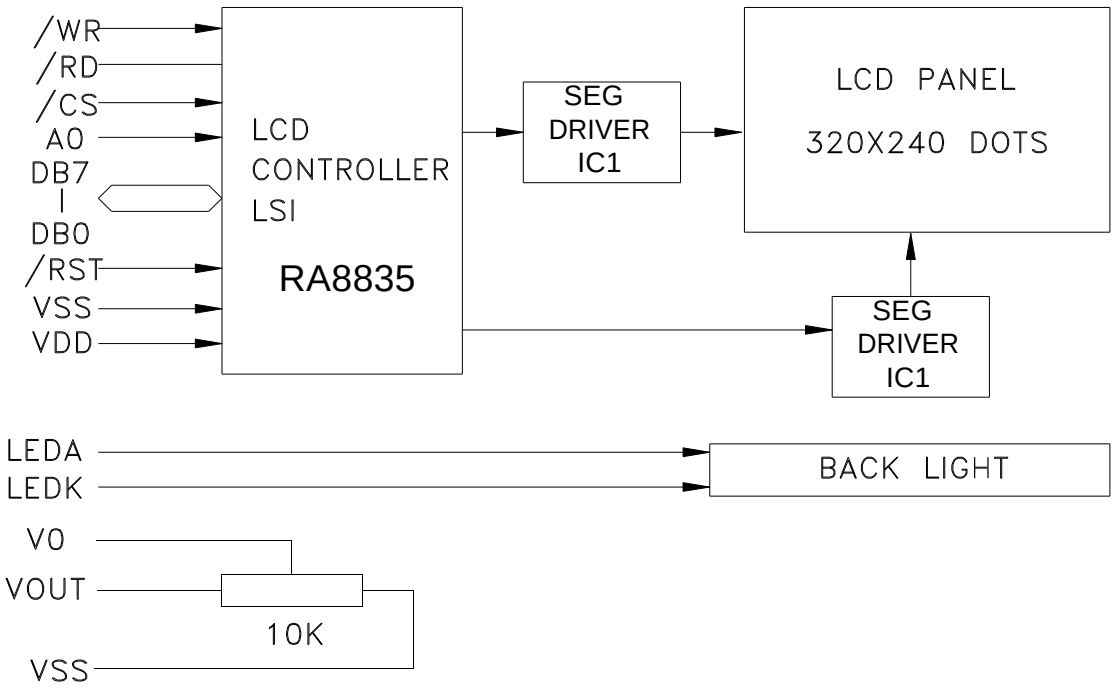
STORAGE TEMP : -30°C TO +80°C
OPERATING TEMP : -20°C TO +70°C
VIEWING DIRECTION : 6 O'CLOCK
DRIVE CONDITION : 1/240DUTY, 1/16 BIAS,VOP=25V
DISPLAY MODE : STN TRANSMISSIVE NEGATIVE(BLUE)
BACK LIGHT ITEM: WHITE I=160mA
LCM OPERATING VOLTAGE5.0V
CONTROLLER/DRIVER IC:RA8835

ICbanQ Inc.

Unspecified Tolerance:	±0.20	UNITS: mm	DATE:	MODE NUMBER :	SHEET: 1 Of 1
DESIGN BY:		WZQ	2012/11/10	HSM320240C-B	
CHECKED BY:					DATE: 2012/11/10
CUSTOM NO:				DO NOT SCALE THIS DRAWING.	PROJECTION

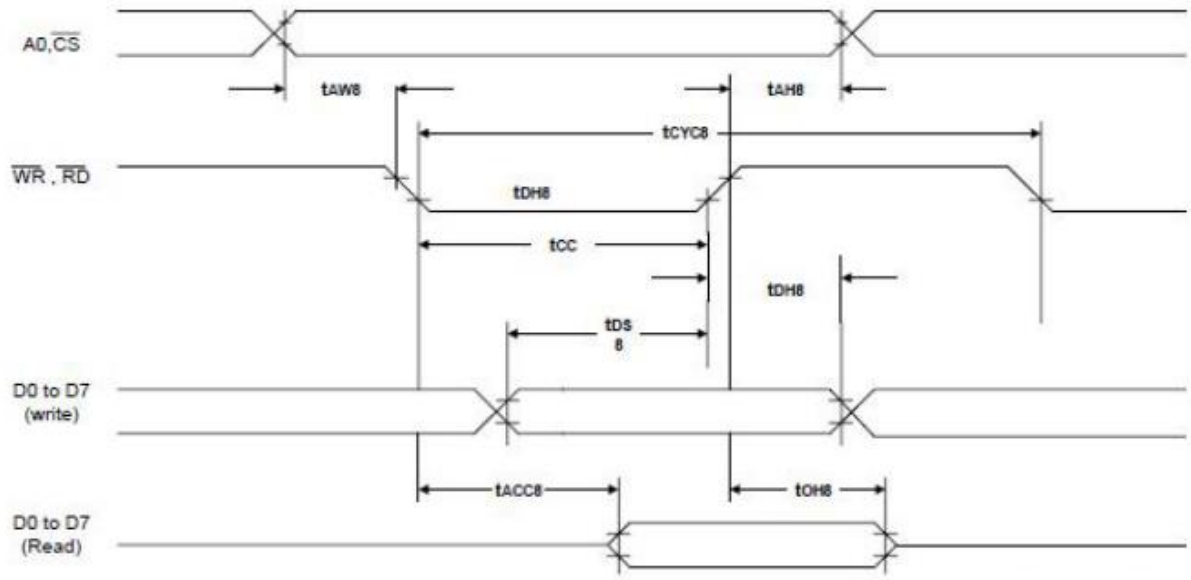
2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VSS	Ground (0V)
2	VCC	Power supply input for driver IC (+5V)
3	VO	LCD driver supply voltages, Contrast Adjust
4	/WR	Write/Read-Write
5	/RD	Enable/Read Enable
6	/CS	L: Chip enable
7	A0	Register/Memory Select
8	/RST	H: Normal L:Initialize
9---16	DB0~DB7	Data bus line
17	LEDA	BACKLIGHT+ （5V）
18	VEE	Negative Voltage output
19	LEDA	BACKLIGHT+ （5V）
20	LEDK	BACKLIGHT- （0V）



2.3 Timing Characteristics

10-3-1 8080 Family Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{CS}$	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
$\overline{WR}$, $\overline{RD}$	t_{CYC8}	System cycle time	note.	—	note.	—	ns	
	t_{CC}	Strobe pulse width	120	—	150	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	$\overline{RD}$ access time	—	50	—	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

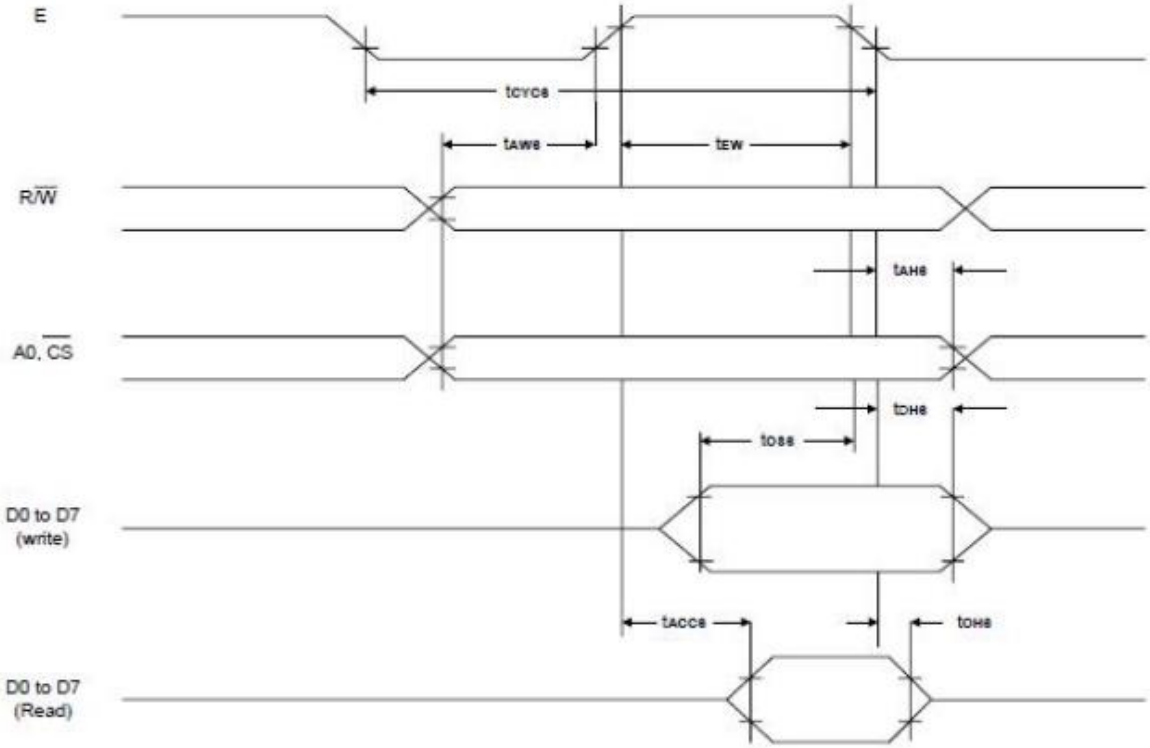
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

10-3-2 6800 Family Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{CS}$, R/(/W)	t_{CYC6}	System cycle time	note.	—	note.	—	ns	CL = 100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	75	ns	
	t_{ACC6}	Access time	—	85	—	130	ns	
E	t_{EW}	Enable pulse width	120	—	150	—	ns	

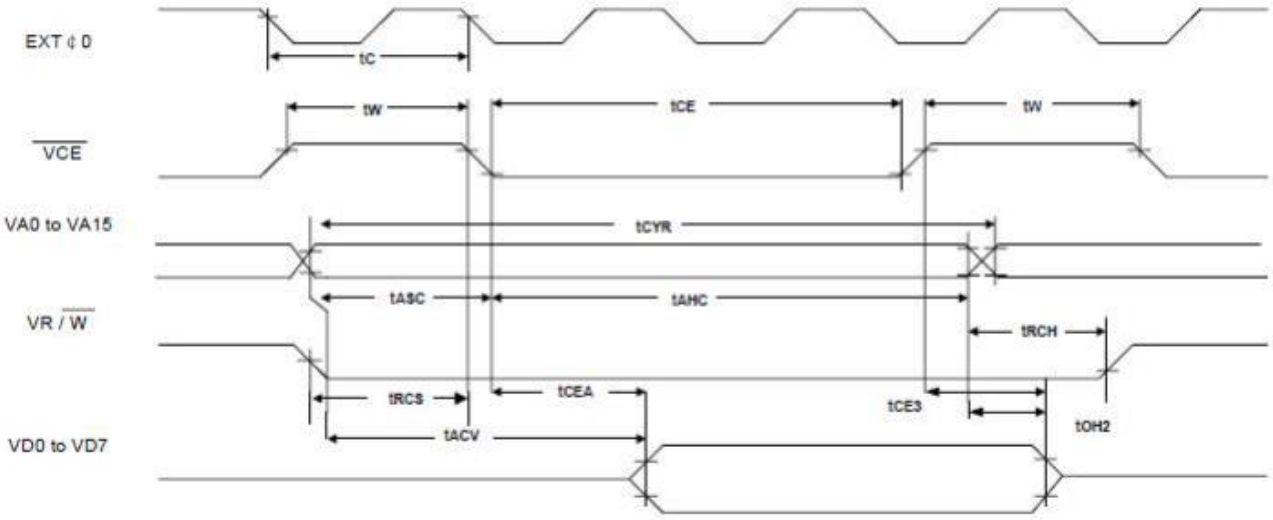
Note: For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

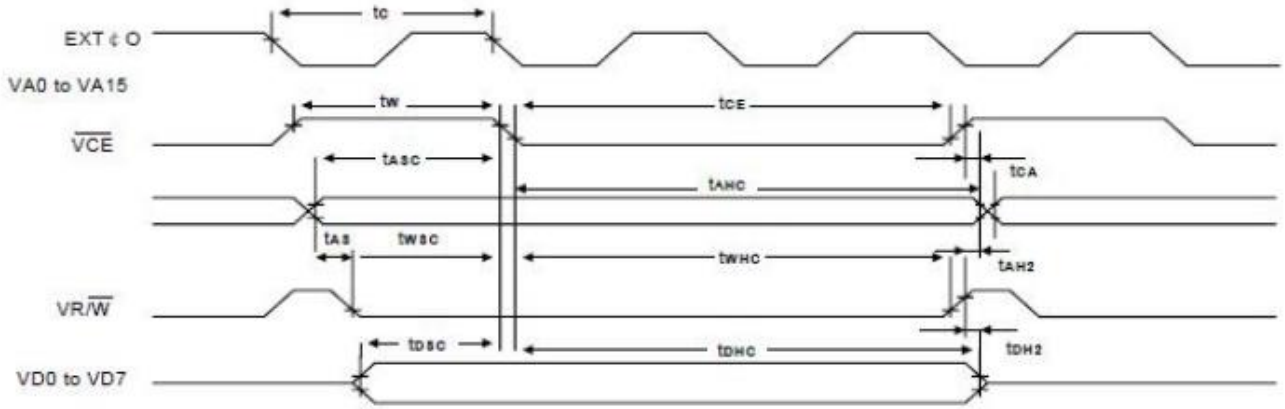
10-3-3 Display Memory Read Timing



Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse width	2t_C – 30	—	2 t_C – 30	—	ns	
VA0 to VA15	t_{CYR}	Read cycle time	3t_C	—	3t_C	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 100	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2 t_C – 30	—	2t_C – 40	—	ns	
$\overline{VRD}$	t_{RCS}	Read cycle setup time to falling edge of $\overline{VCE}$	t_C – 45	—	t_C – 60	—	ns	
	t_{RCH}	Read cycle hold time from rising edge of $\overline{VCE}$	0.5t_C	—	0.5t_C	—	ns	
VD0 to VD7	t_{ACV}	Address access time	—	3t_C – 100	—	3t_C – 115	Ns	
	t_{CEA}	$\overline{VCE}$ access time	—	2t_C – 80	—	2t_C – 90	Ns	
	t_{OH2}	Output data hold time	0	—	0	—	ns	
	t_{CE3}	$\overline{VCE}$ to data off time	0	—	0	—	ns	

10.3-4 Display Memory Write Timing



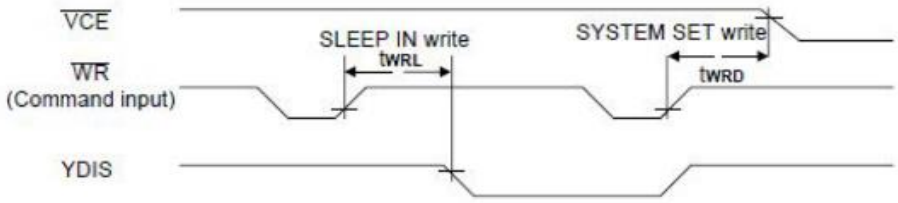
Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse width	$2t_C$ – 30	—	$2t_C$ – 30	—	ns	
VA0 to VA15	t_{CYW}	Write cycle time	3tC	—	$3t_C$	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	$2t_C$ – 30	—	$2t_C$ – 40	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 110	—	ns	
	t_{CA}	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	t_{AS}	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	t_{AH2}	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	t_{WSC}	Write setup time to falling edge of $\overline{VCE}$	t_C – 80	—	t_C – 115	—	ns	
	t_{WHC}	Write hold time from falling edge of $\overline{VCE}$	$2t_C$ – 20	—	$2t_C$ – 20	—	ns	

VD0 to VD7	t_{DSC}	Data input setup time to falling edge of $\overline{VCE}$	t_C – 85	—	t_C – 125	—	ns	
	t_{DHC}	Data input hold time from falling edge of $\overline{VCE}$	$2t_C$ – 30	—	$2t_C$ – 30	—	ns	
	t_{DH2}	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

10-3-5 Sleep In Command Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
$\overline{WR}$	t_{WRD}	$\overline{VCE}$ falling-edge delay time	note 1.	—	note 1.	—	ns	CL = 100 pF
	t_{WRL}	YDIS falling-edge delay time	—	note 2.	—	note 2.	ns	

Notes:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C$. [TC/R] . [L/F] + 70

7-8 Reset

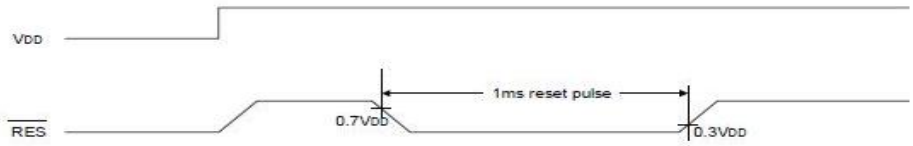


Figure 7-8: Reset Timing

The RA8835 series requires a reset pulse at least 1 ms long after power-on in order to re-initialize its internal state. For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the RA8835 series is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

The RA8835 series cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals XD, LP and FR are halted. A delay of 3 ms (maximum) is required following the rising edges of both $\overline{RES}$ and VDD to allow for system stabilization.

10-2 DC Characteristic

V_{DD} = 2.7 to 5.5V, V_{SS} = 0V, Ta = –20 to 75℃

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	V
Supply voltage	V_{DD}		2.7	3.3/5.0	5.5	V
Register data retention voltage	V_{OH}		2.0	—	6.0	V
Input leakage current	I_{LI}	VI= VDD. See note 5.	—	0.05	2.0	µA
Output leakage current	I_{LO}	VI= VSS. See note 5.	—	0.10	5.0	µA
Operating supply current	Iopr	See note 4.	—	11	15	mA
Quiescent supply current	I_Q	Sleep mode, VOSC1= V($\overline{CS}$)= V($\overline{RD}$)= VDD	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 6.	1.0	—	18.0	MHz
External clock frequency	f_{CL}		1.0	—	10.0	MHz
Oscillator feedback resistance	Rf		0.5	1.0	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	$0.5V_{DD}$	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHT}	IOH= –5.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	IOL= 5.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8 V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHC}	IOH= –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	IOH= 1.6 mA. See note 2.	—	—	VSS+ 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	IOL= 6.0 mA.	—	—	V_{SS} + 0.4V	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5 V_{DD}	0.7 V_{DD}	0.8 V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2 V_{DD}	0.3 V_{DD}	0.5 V_{DD}	V

Notes:

1. D0 to D7, A0, ($\overline{CS}$), ($\overline{RD}$), ($\overline{WR}$), VD0 to VD7, VA0 to VA15, ($\overline{VRD}$), ($\overline{VWR}$) and ($\overline{VCE}$) are TTL-level inputs.
2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.
3. $\overline{RES}$ is an Schmitt-trigger input. The pulse width on ($\overline{RES}$) must be at least 200us. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.

4. f_{OSC} = 10 MHz, no load (no display memory), internal character generator, 256x200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
6. Because the oscillator circuit input bias current is in the order of uA, design the printed circuit board so as to reduce leakage currents.

V_{DD} = 2.7 to 4.5V, V_{SS} = 0V, Ta = –20 to 75℃

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	V
Supply voltage	V_{DD}		2.7	3.5	4.5	V
Register data retention voltage	V_{OH}		2.0	—	6.0	V
Input leakage current	I_{LI}	$V_I = V_{DD}$. See note 5.	—	0.05	2.0	µA
Output leakage current	I_{LO}	$V_I = V_{SS}$. See note 5.	—	0.10	5.0	µA
Operating supply current	Iopr	V_{DD} = 3.5 V. See note 4.	—	3.5	—	mA
		See note 4.	—	—	7.0	
Quiescent supply current	I_Q	Sleep mode, $V_{OSC1} = V_{CS} = V_{RD} = V_{DD}$	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 6.	1.0	—	8.0	MHz
External clock frequency	f_{CL}		1.0	—	8.0	MHz
Oscillator feedback resistance	Rf		0.7	—	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.5 V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHT}	I_{OH} = –3.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 3.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8 V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	V_{SS} + 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	I_{OL} = 6.0 mA.	—	—	V_{SS} + 0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5 V_{DD}	0.7 V_{DD}	0.8 V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2 V_{DD}	0.3 V_{DD}	0.5 V_{DD}	V

Notes

1. D0 to D7, A0, ($\overline{CS}$), ($\overline{RD}$), ($\overline{WR}$), VD0 to VD7, VA0 to VA15, ($\overline{VRD}$), ($\overline{VWR}$) and ($\overline{VCE}$) are TTL-level inputs.
2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.
3. $\overline{RES}$ is an Schmitt-trigger input. The pulse width on ($\overline{RES}$) must be at least 200 s. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. f_{osc} = 10 MHz, no load (no display memory), internal character generator, 256 . 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
6. Because the oscillator circuit input bias current is in the order of μA, design the printed circuit board so as to reduce leakage currents.

2.4 Instruction Table

Table-1: Command Set

Class	Command	Code											Hex	Command Description	Command Read Parameters	
		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			No. of Bytes	Section
System Control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	9-2-1
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	9-2-2
Display Control	DISPLAY ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	9-3-1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	9-3-2
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	9-3-3
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	9-3-6
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	9-3-4
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	9-3-7
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	9-3-5
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	9-r1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	9-4-2
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	9-5-1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	9-5-2

Notes:

1. In general, the internal registers of the RA8835 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged. 2-byte parameters (where two bytes are treated as 1 data item) are handled as follows:

    a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.

    b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

2.5 Inspection Specification

◆Inspection Standard : MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ .

◆Equipment : Gauge、MIL-STD、Powertip Tester、Sample

◆Defect Level : Major Defect AQL 0.4; Minor Defect AQL 1.5 .

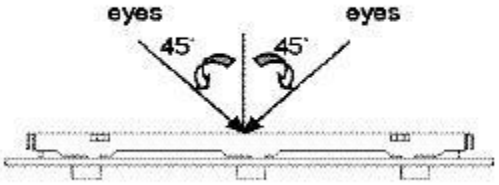
◆OUT Going Defect Level : Sampling .

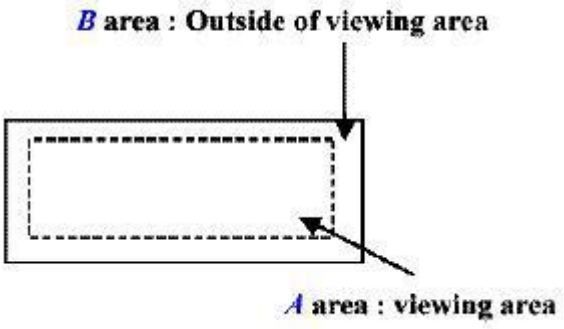
◆Manner of appearance test :

(1). The test be under 40W×2 fluorescent light ' and distance of view must be at 30 cm.

(2). The test direction is base on about around 45° of vertical line. (Fig. 1)

(3). Definition of area . (Fig. 2)

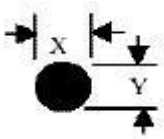


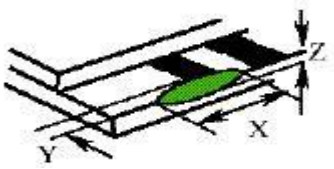


◆ Specification:

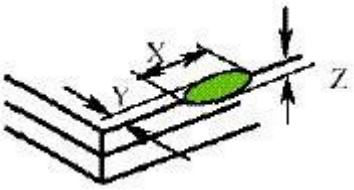
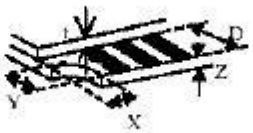
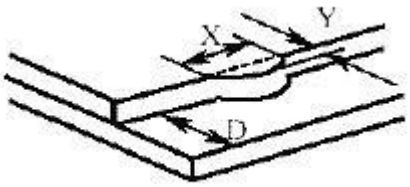
NO	Item	Criterion	level
01	Product condition	1.1 The part number is inconsistent with work order of Production.	Major
		1.2 Mixed production types.	Major
		1.3 Assembled in inverse direction.	Major
02	Quantity	2.1 The quantity is inconsistent with work order of production.	Major
03	Outline dimension	3.1 Product dimension and structure must conform to Structure diagram.	Major
04	Electrical Testing	4.1 Missing line character、dot and icon.	Major
		4.2 No function or no display.	Major
		4.3 Output data is error.	Major
		4.4 LCD viewing angle defect.	Major
		4.5 Current consumption exceeds product specifications.	Major
05	Black or white dot、scratch、contamination Round type	5.1 Round type: 5.1.1 display only : ・White and black spots on display ≦ 0.25mm, no more than Four white or black spots present. ・Densely spaced : NO more than two spots or lines within 3mm	Minor

◆Specification :

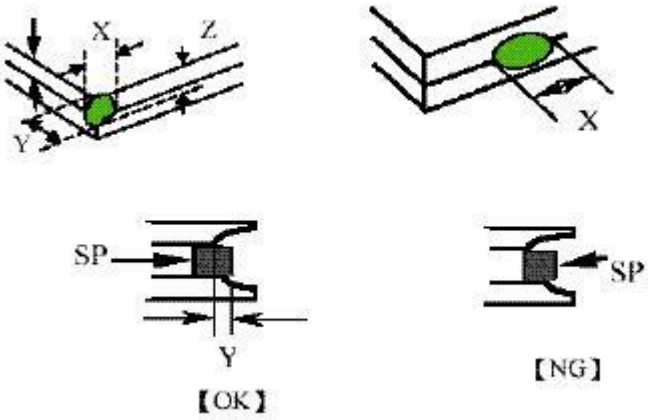
NO	Item	Criterion	level
05	Black or white dot、scratch、contamination Round type  Φ=(x+y)/2  	5.1.2 Nom-display : Dimension (diameter : Φ) Acceptance(Q'ty) Φ≦0.10mm Accept no dense 0.10mm＜Φ≦0.20mm 3 0.20mm＜Φ≦0.25mm 2 Total 4 5.1.3 Line type: Dimension (diameter : Φ) Acceptance (Q'ty) Length width A area B area --- w≦0.03mm Accept no dense Don't count L≦3.0mm 0.03mm＜ [illegible] 4 Don't count L≦2.5mm 0.05mm＜ [illegible] Don't count --- w＞0.075mm As round type	Minor

06	Polarizer Bubble	Dimension (diameter : Φ) Acceptance(Q'ty) A area B area Φ≦0.20mm Accept no dense Don't count 0.20mm＜Φ≦0.50mm 3 Don't count 0.50mm＜Φ≦1.00mm 2 Don't count Φ＞1.00mm 0 Don't count Total quantity 4 Don't count	Minor
07	The crack of glass	● Glass Crack: 7.1 Crack on the circuit of electrode terminal :  X Y Z Front X≦1/5a Y≦1/2D Z≦t Back Neglect	Minor

◆Specification :

NO	Item	Criterion	Level
07	The crack of glass X: The length of Crack Y: The width of crack Z: The thickness of crack D: terminal length T: The thickness of glass A : The length of glass	⬬Glass Crack: 7.2 General glass crack and corner edge: 7.2.1  X Y Z Neglect Out A area Neglect 7.2.2  X Y Z Neglect Out A area Neglect	Minor
		7.3 Glass remain:  X Y Neglect ≦ 1/3 d	Minor

◆Specification :

NO	Item	Criterion	Level
07	The crack of glass X: The length of Crack Y: The width of crack Z: The thickness of crack D: terminal length T: The thickness of glass A : The length of glass	7.4 Corner crack and medial crack:  X Y Z ≦1/5a Crack can't enter viewing area ≦1/2t ≦1/5a Crack can't exceed the half of width of SP width of SP 1/2t<Z≦2t	Minor
08	Backlight elements	8.1 Backlight can't work normally.	Major
		8.2 Backlight doesn't light or color is wrong.	Major
		8.3 Illumination source flickers when lit.	Major
09	General appearance	9.1 pin type must match type in specification sheet	Major
		9.2 No short circuits in components on PCB or FPC	Major
		9.3Product packaging must the same as specified on packaging specification sheet.	Major
		9.4 The folding and peeled off in polarizer are not acceptable	Major
		9.5 The PCB or FPC between B/L assembled distance (PCB or FPC) is ≦1.5mm	Major